DEVELOPING RADIATION HARDENING BY DESIGN METHODOLOGIES FOR SINGLE EVENT MITIGATION IN SILICON-GERMANIUM BICMOS TECHNOLOGIES

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DEVELOPING RADIATION HARDENING BY DESIGN METHODOLOGIES FOR SINGLE EVENT MITIGATION IN SILICON-GERMANIUM BICMOS TECHNOLOGIES

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To Elizabeth:

Older Sister, Role Model, Personal Hero

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SUMMARY

This work presents a summary of two new radiation hardening by design methodologies which are being investigated as a means of mitigating single event effects in SiGe BiCMOS technologies. In Chapter 1, Silicon-Germanium technology is introduced as a viable technology platform for incorporation in extreme environments, especially those encompassing low temperatures and large radiation fields (space). An overview of the technology is presented, including a description of the performance optimizations achieved by practicing bandgap engineering in a silicon system. SiGe technology is shown to be inherently conducive for low temperature operation; however, a range of degrading radiation effects can wreak havoc on this technology.

Chapter 2 introduces the various radioactive particles and sources which exist in the space environment. This environment is shown to be extremely dynamic, requiring extensive knowledge of solar cycles, orbital altitudes, mission paths, and mission durations before any prediction of the encountered radation environment can be made. The interaction of radiation with microelectronic systems is broken down into three different catergories of effects. The impact of these effects on SiGe technology is outlined, revealing a suceptibility of the technology to single event effects. The current radiation hardening methodologies for SiGe systems to single event effects is breifly reviewed, stressing the significant area and power penalties which accompany these designs. These drawbacks motivate the needs to investigate new hardening methodologies which have little to no system penalties.

Chapter 3 introduces the first radiation hardening by design technique, specifically the reduction/removal of deep trench isolation from a SiGe BiCMOS platform. Although DTI provides excellent electrical isolation and reduced capacitive parasitics, it

is shown that charge collection events for strikes within the active area of the device is increased as a result of charge confinement from the DTI. If the DTI is eliminated, more charge is able to diffuse away from the sensitive subcollector-substrate junction and recombine in the substrate. These results are determined from heavy ion microbeam data, coupled with full 3-D TCAD simulations. Additionaly, no total dose degradation is shown to be experienced by varying the deep trench depth through experimental data obtained from 10 keV X-ray and 63 MeV proton radiation. Despite this benefit, an increase in charge collection is found for ion strikes outside the active area of the device. To mitigate this charge collection, it is proposed that junction isolation be employed. The studies from this chapter have been published in [31].

In Chapter 4, an entirely new device design is introduced as a possible means of providing single event immunity. The device is called the inverse-mode cascode SiGe HBT, and its fabrication and operation are breifly outlined. The ability of the device to decouple the output terminal from the sensitive buried subcollector-substrate junction is highlighted as a possible means to eliminate suceptibility to single event effects. The device is experimentally anaylzed in both a TID and SEE context using a 10 keV X-ray as well as a heavy ion microbeam. By coupling the experimental results with 3-D TCAD simulations, the charge collection physics of this new structure are analyzed. It is found that providing an electrically conductive path from the subcollector to a rail will siginificantly improve the charge collection statistics of the device.

Finally, Chapter 5 concludes this thesis with a review of the topics discussed in Chapters 1, 2, 3, and 4. Additionally the future directions to be taken with these radiation hardening methodologies are outlined. Before they can be accepted as successful techniques, bit error rate testing on digital circuit applications must be performed and compared to unhardened architectures.

CHAPTER I

SIGE HETEROJUNCTION BIPOLAR TRANSISTORS: COMPOSITION, OPERATION, AND EXTREME ENVIRONMENT COMPATIBILITY

1.1 Introduction

A brief introduction to Silicon-Germanium technology is introduced in this chapter, encompassing its material composition, operational performance enhancements, and ability to be integrated in applications functioning in extreme environments. The motivation for applying this aggressive technology in space applications is initially given and the need for investigating radiation hardening by design methodologies is highlighted. The practice of bandgap engineering to form a competitive heterojunction bipolar transistor (HBT) is then discussed and the resulting device performance enhancements are introduced.

1.2 Motivation

The advent of the integrated circuit (IC) has spurred a technological revolution which has reshaped countless aspects of the lives of individuals across the globe. As technology scaling on both bipolar and field-effect transistors has matured from discrete components to very large scale integration (VLSI) on a single semiconductor wafer, the possibility for system on a chip (SoC) solutions has emerged, fueling the markets for analog/mixed signal, radio frequency, mm-wave, and wired/wireless high speed communications applications. A bounty of semiconductor technologies have emerged as contenders for employment in these applications (including but

not limited to III-V, silicon-on-sapphire, silicon-on-insulator, RFCMOS, and Silicon-Germanium) each boasting their own characteristic strengths and weaknesses. As system specifications become increasingly stringent, the need for improved device metrics matching the requirements of a specific application, becomes increasingly important. This is especially essential for niche markets that have highly specific needs and generally operate in unique environmental conditions. One such niche market which is becoming increasingly important (and challenging) is that of extreme environments.

Extreme environments encompass the operation of electronic systems in surroundings which exist outside of the domain of standard commercial or military specifications [7]. These environments can include any combination of extreme high/low temperatures, large amounts of mechanical stress, chemical corrosion, or intense radiation fields. One market that encounters many of these environmental extremes is space-borne electronic systems. Space is a very diverse, hostile environment whose surroundings vary greatly upon the type of application being pursued. Temperatures can vary from cryogenic (deep-space probes) to extremely high (illuminated lunar craters) and radiation levels are highly dependent on the altitude from the earth's surface. Any technology to be used in these applications must be tolerant to both temperature and radiation induced effects. Silicon-germanium technology has arisen as suitable platform for incorporation in space-based electronic systems given its high speed, low cost, compatibility with best-of-breed silicon CMOS technology, and intrinsic excellent low temperature performance. The radiation response of silicon-germanium devices (specifically the occurrence of single event effects) and methods to harden the technology to these degrading effects is still an on-going area of research.

Radioactive particles in space originate from numerous sources, including particles ejected from the corona of the sun (solar winds), charged particles trapped in the magnetic fields of large solar bodies, and the ever present background of galactic

cosmic rays (a cosmic stew of extremely high energy ions, protons, and photons) [34]. The Van Allen belts, consisting of energetic protons and electrons that have become trapped by the earth's internal magnetic field, are of particular concern for orbital applications [20]. Any electronic system which operates while being exposed to these sources is liable to suffer from a broad range of detrimental effects. These effects include displacement damage of the bulk semiconductor material, ionization damage in the oxides of the semiconductor and oxide-semiconductor interfaces, and finally a compendium of single event effects (SEE). As semiconductor technologies continue to mature with increasing device scaling, radiation susceptibility becomes an increasing concern for reliable operation in space environments.

Silicon-germanium heterojunction bipolar transistors (SiGe HBTs) have been repeatedly shown to be inherently resilient to total ionizing dose and displacement damage [37, 36, 3, 19], while significant vulnerability to SEEs has been identified [33, 17, 16, 35]. To address this sensitivity, radiation hardening mechanisms employed on both the device and circuit architecture levels are being investigated. The most common hardening methodologies encountered are radiation hardening by process (RHBP), which entails modifications to fabrication steps (additional masks), and radiation hardening by design (RHBD), which involves alterations to circuit architectures or changes to device structure which doesn't interrupt normal fabrication flow. Given that RHBP can be extremely costly and forces a foundry to break away from their process of record, it is highly desirable to pursue RHBD techniques that achieve acceptable levels of radiation tolerance while maintaining low system costs.

1.3 Silicon-Germanium BiCMOS Technology

Silicon semiconductor technology has dominated the commercial IC sector for many years, largely driven by mature fabrication processes, low-cost, and the ability to generate high-yield wafers. Although the performance of these transistors severely

lagged behind other technologies (such as III-V), the traditional practice of integrating separately packaged, application-specific ICs together to form a full system has allowed silicon ICs to be employed for components which are compatible with the mediocre performance of pure silicon transistors. However, with the push towards developing SoC solutions, entire systems must be implemented on a single semiconductor wafer, requiring the material to provide all of the necessary performance metrics needed for every system component. With silicon's poor carrier mobilities and relatively low saturation velocity under high electric field conditions, the technology is unable to achieve device speeds necessary for RF and microwave circuit components [32]. At the same time, although III-V technology can achieve the desired device speeds for these applications, the difficulties in achieving large, highly-integrated, high-yield wafers results in much higher costs. An optimal solution would combine the performance of III-V technology with standard silicon's ease of fabrication, high-integration capability, and low cost. Silicon-germanium technology has arisen as a candidate for marrying the benefits of both III-V and intrinsic silicon devices into a single competitive solution for RF, mm-wave, microwave, and digital SoC applications.

The concept of incorporating germanium into a silicon material system is far from new, and was actually first conceptualized by William Shockley in the days of the primitive transistor. Despite its early origins, the reality of silicon-germanium alloys would not manifest itself until several decades later, once processing technology evolved to allow device-suitable films to be manufactured. Today, ultra-high vacuum chemical vapor deposition (UHV/CVD) and molecular beam epitaxy (MBE) provide the process techniques necessary to grow extremely thin, defect-free SiGe films. Given the lattice mismatch between a SiGe alloy (exact value dependent on the germanium fraction following Vegard's rule [9]) and a Si substrate, SiGe films will experience biaxial compressive strain to adopt the same crystalline structure as the underlying Si material. If film thicknesses exceeds a specified value (termed critical thickness, calculated from

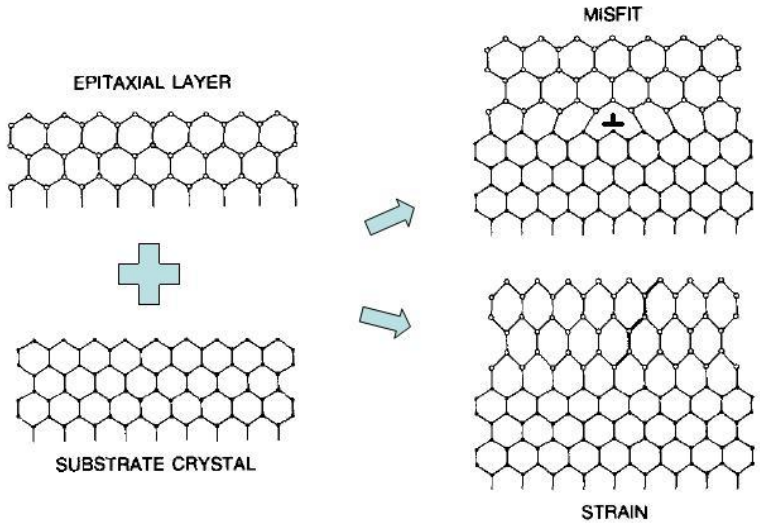

Figure 1.1: A conceptual representation of two possible outcomes for lattice mismatched epitaxial growth: a strained layer or a relaxed layer with misfit dislocations. (After [4])

several variables including total germanium content and buffer layer thicknesses), films will relax forming misfit dislocations within the film that are unsuitable for transistor operation as illustrated in Figure 1.1. Replacing the base region of a standard Si BJT with this thin SiGe film essentially forms the silicon-germanium heterojunction bipolar transistor. This device can be integrated with standard CMOS fabrication, with minimal increase to mask layers, to form a hybrid SiGe BiCMOS platform that allows IC designers to take advantage of both high-performance bipolar and highly-integrated Si CMOS.

1.3.1 Silicon Bandgap Engineering

The growth and inclusion of a SiGe film in a silicon transistor represents the first successful attempt at bandgap engineering in a silicon system. When comparing silicon and germanium as bulk materials, it is evident that germanium has many material properties superior to that of pure silicon as shown in Table 1.1. Intuitively, it is expected that mixing these two elements will result in an alloy whose material

Table 1.1: Device-relevant material parameters for both bulk silicon and germanium (After [32]).

Parameter	Silicon	Germanium	Units
E_g	1.12	0.66	eV
m_n^*/m_o	1.18	0.55	–
m_p^*/m_o	0.81	0.36	–
μ_n	1350	3900	$cm^2/V\times$s
μ_p	480	1900	$cm^2/V\times$s
a	5.43	5.66	Å

properties are more desirable than pure silicon. Through the inclusion of germanium in a silicon system, devices can be tailored to improve their performance by adjusting a variety of operational characteristics. Given that germanium has an intrinsically smaller bandgap than silicon, it is expected that a SiGe film will also have a smaller bandgap. By replacing the base of a standard Si bipolar transistor with a strained SiGe alloy (physically consisting of a SiGe alloy sandwiched between two intrinsic silicon layers), a type-I energy band alignment is obtained, where the band edges of the SiGe material are contained with the silicon band edges as shown in Figure 1.2.

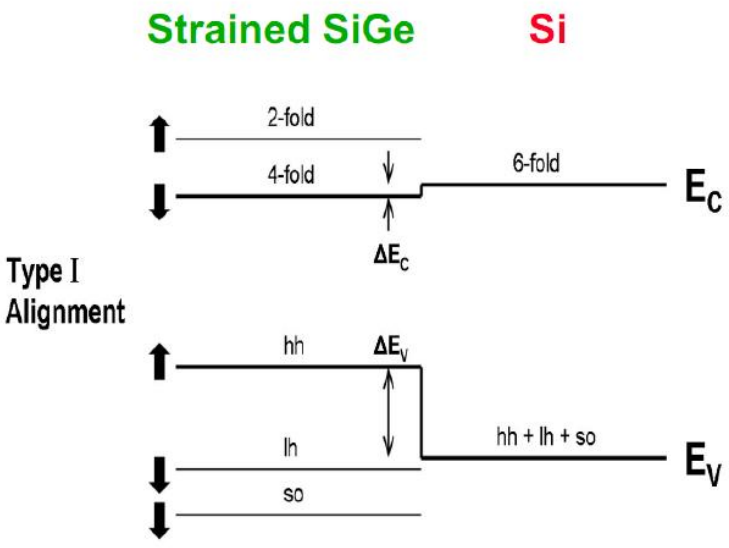

Figure 1.2: Band alignments of a strained SiGe alloy grown on a silicon wafer. The break in band degeneracies as well as the offsets in band edges is highlighted. (After [9])

As can be seen from the figure, the dominating offset is the discontinuity in the valence bands (E_V), which is highly desirable. Additional effects induced by the compressively strained SiGe layer include a break in the band degeneracies, an increase in majority-carrier hole mobility (for p-type material), a decrease in minority carrier electron mobility (p-type material), and a decrease in the density of carrier states (N_C and N_V).

An addition tuning knob for optimization of device performance metrics of a SiGe HBTs at an engineer's disposal is the grading profile of germanium used in the design. Graded germanium in the base of an HBT will result in a graded bandgap throughout the base, which will manifest itself in the conduction band of the energy band diagram of the HBT. The translation from an initial valence band offset to a conduction band offset in the complete energy band diagram can be understood through the following discussion. Given that the p-doping in the base is constant, the Fermi level and the difference between the Fermi level and valence bend are fixed. Also, the transistor is in a state of equilibrium, forcing the Fermi level to be constant. To accommodate these conditions, while maintaining the reduction in badgap with graded germanium, the conduction band is forced to change. An illustrative energy band diagram for a graded germanium SiGe HBT operating in forward active mode is shown in Figure 1.3.

In addition to the normal band bending present in forward-active mode, an addition bend in the conduction band is present in the neutral base region, as a result of the germanium grading effect, discussed previously. Recalling the interrelationship between band-bending and electric fields as described by Equation 1.1, it becomes evident that an additional drift field will be present in the base which will boost device performance.

$$\varepsilon = -\frac{dV}{dx} = \frac{d(\frac{-(E(x)-E_{ref}(x))}{q})}{dx} \tag{1.1}$$

Specifically, this inherent drift field will accelerate minority carrier electrons across the base, reducing the base transit time which has classically been the metric dominating

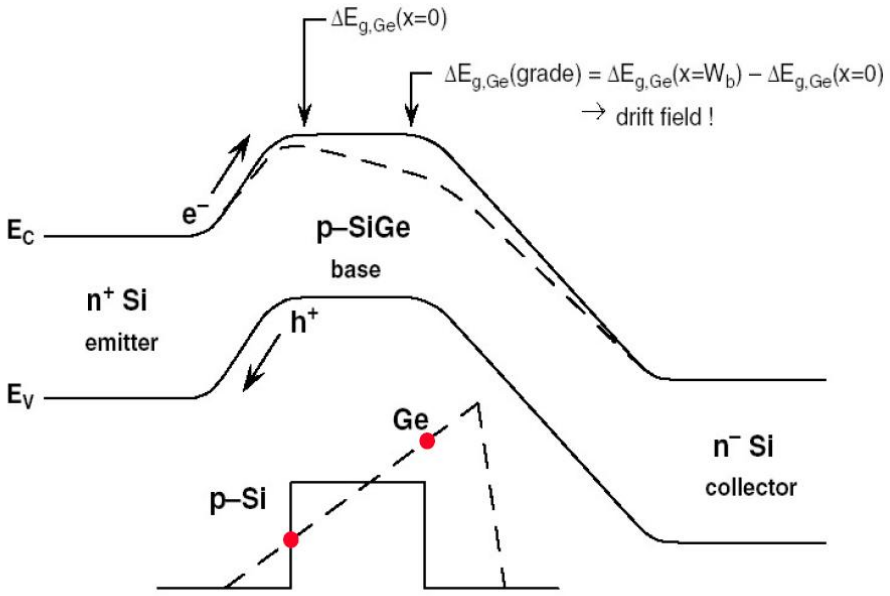

Figure 1.3: Energy band diagram of an NPN SiGe HBT operating in forward active mode Germanium-induced effects are highlighted on the energy band diagram (After [9]).

maximum operating frequencies of devices. The band offset at the emitter-base junction will also provide device performance enhancement, boosting the collector current of the device while maintaining the same base current, thereby increasing device gain. For a full discussion of the impact and benefits of a graded germanium base profile on device physics, the reader is directed to [8].

CHAPTER II

RADIATION SOURCES IN SPACE AND THEIR EFFECTS ON SIGE TECHNOLOGY

2.1 Introduction

This chapter will introduce the harsh radiation environment present in space, and its detrimental effects on microelectronic systems which operate in these conditions. The first section explores the sources of radioactive particles in space in addition to discussing their elemental compositions and relative risks to space missions. In the next section, a breakdown of the various effects on SiGe technologies due to these sources is presented. Total ionizing dose and displacement damage are briefly discussed, with more emphasis being placed on understanding single event effects; motivating the need for hardening mechanisms to mitigate these effects. Finally, an overview of past literature is presented in the context of radiation hardening by process (RHBP) as well as radiation hardening by design (RHBD) on SiGe HBTs.

2.2 Space-based Radiation Sources

The serene night sky seen from the surface of the earth is misleading in terms of the actual environment that exists in space. Above the earth's protective atmosphere the sky is reeling with highly energetic particles that are extremely harmful for both humans and electronic systems. To complicate matters further, the radiation environment of space is also incredibly dynamic. The exact environment encountered for an application on a given space mission is dependent on numerous variables including the current solar cycle, the orbital path and altitude of a craft, and the duration of the orbit. The possible earth orbits can be broken down into four categories:

low earth orbit (LEO), below an altitude of 10,000 km, medium earth orbit (MEO), between 10,000 to 20,000 km, geostationary orbit (GEO) at 36,000 km, and highly elliptical orbit (HEO) [21]. Each orbit is subject to various particle sources, types, and intensities. To insure that our satellites and other spacecraft are operational in this extremely harsh environment, a detailed understanding of the various sources of space radiation and their interactions with microelectronic systems is necessary.

2.2.1 Van Allen Radiation Belts

The Van Allen radiation belts arise from the magnetosphere of the earth, which traps charged particles ejected from the sun (solar winds) forming a plasma torus around the earth as seen in Figure 2.1. These belts are composed of trapped electrons, protons and low energy heavy ions that gyrate around and traverse along magnetic field lines. Of predominant concern for orbital electronics are the trapped electrons and protons,

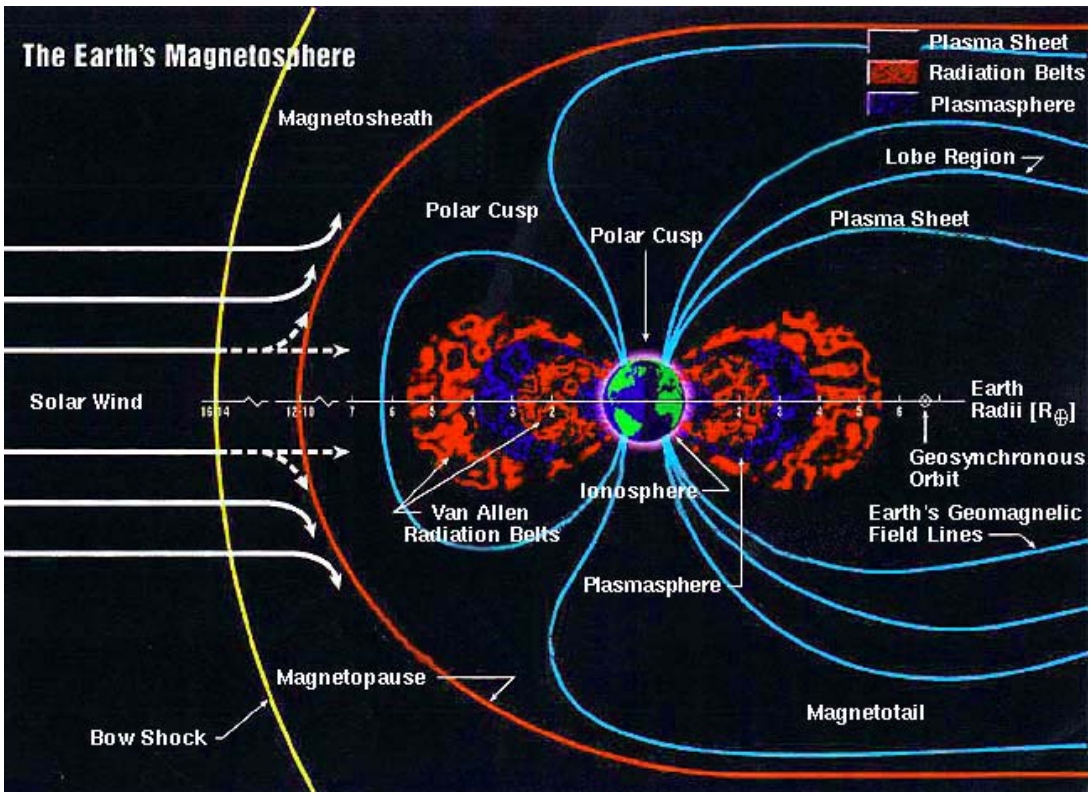

Figure 2.1: Van Allen belts surrounding the earth, fueled by solar winds and held in place by the earth's magnetic field (After [25]).

which can have very large energies (the low energy heavy ions can be blocked with minimal shielding). The electrons of the Van Allen belts can be broken into two zones, the inner zone and the outer zone. The inner zone extends outwards to about 2.4 earth radii, and is composed of a spectra of lower energy electrons (<5 MeV); meanwhile, the outer zone (beginning at 2.8 earth radii and stretching out to 12 earth radii) has an energy spectra that extends up to 7 MeV [34]. Unlike electrons, trapped proton distributions can not be broken into zones, given that their spatial coordinates vary inversely with their energy as seen in Figure 2.2. Proton energies can extend from several hundred MeV close to the earth's atmosphere to a few MeV on the outer edges of the Van Allen belts. The relative fluxes of the particles in these belts are strongly dependent on the current solar cycle and altitude.

A troublesome characteristic of the Van Allen radiation belts is the presence of the South Atlantic Anomaly (SAA) [21]. The SAA is a depression in the earth's magnetic field, over the north eastern coast of South America. Trapped particles contained

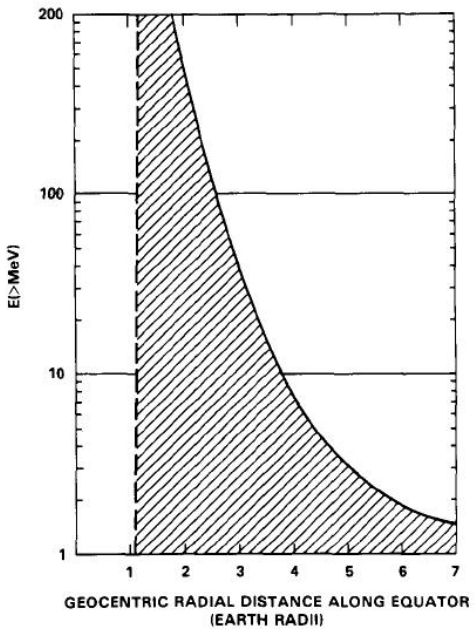

Figure 2.2: Energy of trapped protons as a function of distance from the earth's surface (After [34]).

within the SAA are the closest to the earth's atmosphere than any other particle in the Van Allen belts. These particles (particularly the very high energy protons which are characteristically close to the earth's atmosphere) are of particular concern for LEO applications that pass through this region of space [34]. The SAA is another demonstration of the importance of understanding every aspect of an orbital mission before a prediction of the total radiation environment encountered can be made.

2.2.2 Transiting Radiation

The other spectrum of radioactive particles in space includes un-trapped radiation which is traversing through space. This radiation originates from ejected particles from the sun's corona (solar flares) and galactic cosmic rays [34]. Both radiation sources are primarily composed of high energy protons, high energy protons, and photons. Solar flares are a periodic occurrence which corresponds to the solar cycle (peaking at a solar maximum); however, galactic cosmic rays are an ever present threat to electronic systems operating in GEO, HEO, or deep space (systems operating in LEO to MEO are generally shielded from these highly energetic transiting particles by the geomagnetic field of the earth). The source of galactic cosmic rays is a disputed topic, but was traditionally believed to be remnants of supernova explosions [23]. Despite controversy over their origins, the compositions and energy spectra of galactic cosmic rays are well understood (which is of utmost importance to a radiation effects engineer!). The relative distribution of elements in galactic cosmic rays based on their atomic charge is shown in Figure 2.3. These particles typically have energies which peak around 1 GeV/nucleon when they are near the earth. Given their high energies, these particles are deeply penetrating, and sensitive electronics can not be effectively shielded using aluminum plating with reasonable thicknesses.

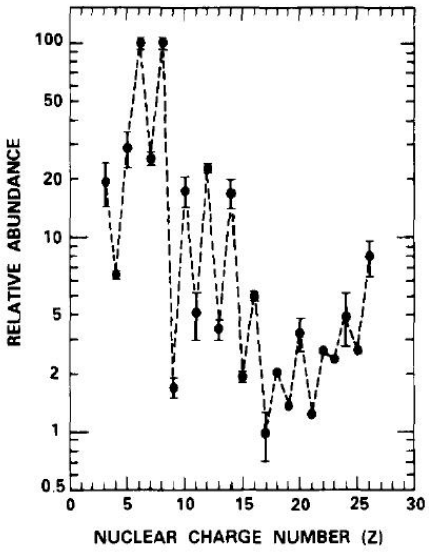

Figure 2.3: Relative distribution of elements contained in galactic cosmic rays (After [34]).

2.3 Radiation Effects in SiGe HBTs

Having established the details of the various radiation components in a space environment, it is logical to next move into a discussion of the impact of these sources on microelectronic systems which operate in these environments. Although the focus will be on radiation effects in a SiGe bipolar system, the importance of understanding the effects on all system components should not be disregarded. The effects of radiation on SiGe HBTs can be classified in the following three catergories: (i) ionization damage (total ionizing dose, TID), (ii) displacement damage (DD), and (iii) single event effects (SEE). Comprehensive research has been performed over the decades to understanding and minimizing the detrimental effects associated with TID and DD across a multitude of semiconductor platforms and generations. SiGe technology has been repeatedly shown to be resilient to TID damage, maintaining nominal device operation with minimal degradation at typical bias values [3, 36, 37, 19]. However, SiGe technology has been shown to be quite vulnerable to single event effects [33, 24]. In the following sections the specifics of TID/DD and SEE are presented. Single event

upset is identified as a particular concern in the realm of SEEs, and the physical origin of this effect is discussed. Finally an overview of past research into radiation hardening techniques is provided.

2.3.1 TID/DD

As an energetic ionizing particle (photon, electron, proton, heavy ion, etc.) traverses through a semiconducting/insulating material, it will deposit energy in the system resulting in the ionization of electron/hole pairs. The total amount of energy absorbed by a material is defined as the rad, a material-dependent quantity, and is used to quantify the total ionizing dose received by a material. The rad (radiation absobred dose) is defined as 100 ergs per gram of energy absorbed by a given material and is calculated through Equation 2.1 .

$$rad = LET \times fluence \times 1.60 \times 10^{-5} \tag{2.1}$$

where the LET is a material-dependent variable that quantizes the rate of energy loss of an impingent particle and fluence is the total number of particles striking a material [21].

Depending on the particle type, energy loss is accomplished through various means, including but not limited to: elastic scattering (electrons, protons, and heavy ions), photoelectric effect (photons), and pair production (photons) [6]. In the bulk of a semiconductor material, this ionized charge does not have long-term detrimental affects; however, insulating materials (specifically oxides in a semiconductor system) are susceptible to being damaged by this charge. If an impinging particle has sufficient mass and momentum, it can experience an in-elastic scattering event, where an atom from the semiconductor lattice is physically displaced. This process is termed displacement damage, and occurs for proton, neutron, and heavy ion radiation. The traps formed from these vacancies are dispersed throughout the energy bandgap of the semiconductor and can have a range of effects on the device. These include increases

in resistances from dopant deactivation, reductions in carrier mobility from increased scattering events, increases in leakage currents from thermal carrier generation, and increases in carrier tunneling across barrier due to reductions in potential height and widths [9]. As technologies mature and scale in size, the volumes of transistor active regions shrink, decreasing the effects of displacement damage on a device.

Holes that are created in an oxide material due to ionizing radiation exposure are the primary damaging mechanism for semiconductor technologies. These holes either become trapped within the oxide, forming fixed charges in the oxide bulk, or migrate to oxide-semiconductor interfaces due to electric field lines in the oxide. At the interfaces, holes can interact with dangling oxygen bonds that are passivated with hydrogen, breaking these bonds and forming interface charge traps [27]. These trapped charges and interface states will lead to increases in device leakage (correlating to gain degradation in a bipolar technology). The sensitive oxides for SiGe HBTs include the emitter-base spacer oxide and the shallow trench isolation (STI) oxide, as demonstrated in Figure 2.4.

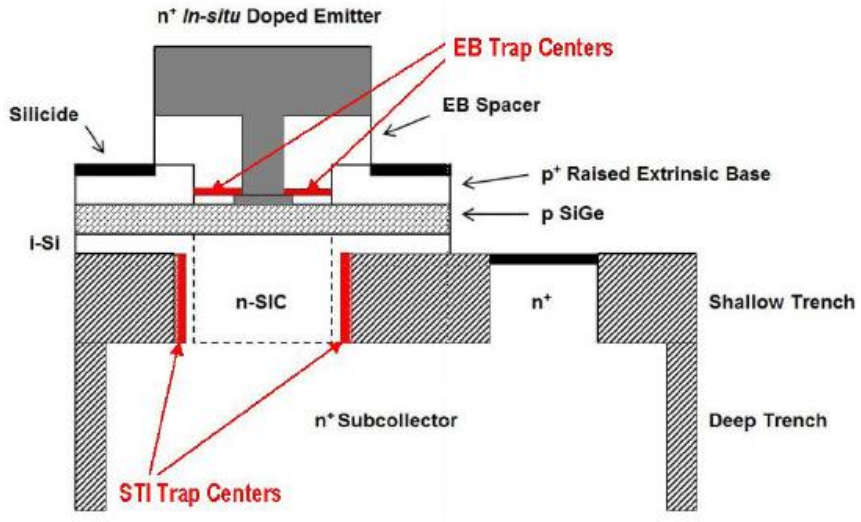

Figure 2.4: Cross section of 3^{rd} generation SiGe platform with sensitive oxides clearly illustrated (After [9]).

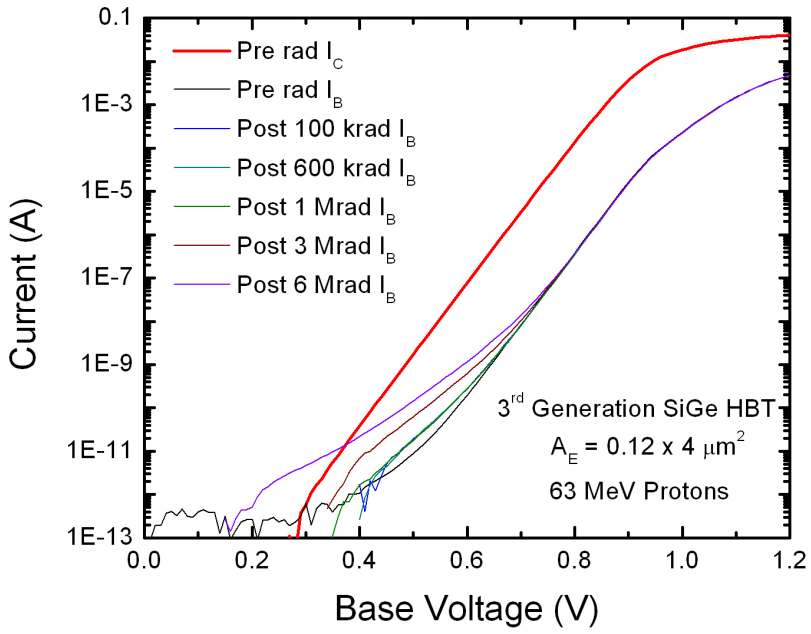

Figure 2.5: Characteristic TID degradation of the low-injection base current resulting from 63 MeV proton exposure.

Given that the emitter-base and base-collector depletion regions overlap these oxides, any traps at the oxide-semiconductor interface (D_{it}) will increase the amount of surface recombination, adding to the base leakage currents and reducing gain. A multitude of TID studies have been performed on multiple generations of IBM's SiGe BiCMOS technology. In addition to varying technology generations, these studies also looked at the impact of different radiation sources, dose rates, and temperatures [36, 37]. Overall SiGe BiCMOS technology is found to be resilient to total dose damage suffering from base leakage currents primarily in low-injection regimes, where devices in circuits are rarely biased. As an example, a representative post 63 MeV proton irradiation gummel plot of a third generation SiGe HBT is shown for various total dose values in Figure 2.5. A gradual rise in base leakage current is evident as the total absorbed dose increases, indicative of an increase in trap density within the sensitive emitter-base spacer oxide. This leakage is only apparent in the low-injection

Table 2.1: Compendium of Single Event Effects.

Acronymn	Effect	Error Type	Sensitive Technologies
SEL	Single Event Latch-up	Hard	Primarily FETs
SEGR	Single Event Gate Rupture	Hard	FETs
SEB	Single Event Burnout	Hard	JFETs, Diodes
SET	Single Event Transient	Soft	HBTs, FETs
SEU	Single Event Upset	Soft	HBTs, FETs
MBU	Multiple Bit Upset	Soft	HBTs, FETs

regime (base bias values <800mV) and quickly falls below the background forward diffusion current for bias voltages above this regime. The robust nature of SiGe HBTs to TID can be attributed to several features of the technology including: their minimal overlap of oxides over sensitive device regions, heavy doping of the extrinsic base, and an oxide/nitride composite composition. As SiGe technology continues to scale and mature, tolerance to both DD and TID will improve, as active volumes and oxides shrink in size.

2.3.2 Single Event Effects

While TID and DD describe accumulated damage to a semiconductor system, SEEs describe transient effects which can either have short or long term consequences. Single event effects encompass a broad range of deleterious errors in a semiconductor system which range from destructive or hard errors to recoverable or soft errors. Despite the wide range of SEEs that exist, each type of error originates from the same phenomena a highly concentrated track of charge pairs generated in the bulk of a device which interact with surrounding depletion regions and electric fields as the free carrier concentration is restored to equilibrium levels. A summary of the different types of errors is provided in Table 2.1. Given that orbital satellite communications encompass high-speed digital logic blocks, the upset of a digital logic state (SEU/MBU) is a foremost concern for satellite system designers. Sensitivities to SEU have been shown to increase as system clocking speeds have increased [5], further motivating the need

to understand and mitigate these errors.

As an energetic charged particle passes through a semiconductor material it deposits energy in the form of ionized charge (electron-hole pairs) along its trajectory, forming a dense track of mobile charge pairs. A metric for describing the amount of energy lost by a particle through a material (and a means for calculating the total charge generated) is the linear energy transfer (LET). The LET of a particle defines the energy loss per unit path length, normalized by the density of the material. The most standard units of LET are $\frac{MeVcm^2}{mg}$. The value of a particle's LET depends on a wide range of parameters including the particle mass, particle energy, and target material. With the LET, the total amount of charge deposited can be calculated, since the energy required to generate a single electron-hole pair is known for a given material target. The density of electron-hole pairs that are generated within the charge track is typically between 10^{18} and 10^{19} cm^{-3}; several orders of magnitude higher than the background doping of the substrate of standard semiconductor technologies [22]. For just a bulk piece of semiconductor material, this charge will diffuse radially outward, through the process of ambipolar diffusion (to maintain neutrality of the charge plasma), until enough recombination events have taken place to restore the free carrier concentration to equilibrium levels. For an IC, which contains devices composed of p-n junctions, there are several different mechanisms which take place aside from ambipolar diffusion to reestablish equilibrium conditions of free carrier concentrations. These other mechanisms can have detrimental affects on the operation of a circuit containing a device which has been struck with an energetic charged particle.

If a particle passes directly through the depletion region of a p-n junction, the deposited charge will result in several different phenomena occurring. First, the electric field lines of the depletion will result in the separation of electron-hole pairs, with electrons drifting towards the n-type material and holes drifting towards the p-type

material. Second, given the large densities of mobile charge carriers generated by an impingent particle, these charges will screen the electric field lines contained within the depletion region. As a result, the depletion region will collapse, and the electric field lines which were initially confined within the depletion region are pushed outwards to maintain the applied voltage across the junction. This distortion of the electric field lines has come to be known as the funnel effect [22, 11, 12] and is illustrated in Figure 2.6. With electric fields stretching deeper into the substrate, a greater amount of deposited charge is collected (a more accurate description is to say charge is induced on terminals) by the contacts on the n and p-type materials. The funneling effect is not limited to only instances where the particle passes directly through a depletion region. Given that substrate dopings are relatively low for most commercial semiconductor technologies ($\approx 10^{14}$ - 10^{15} cm^{-3}), the diffusion length of carriers can be relatively large ($\approx$100 μm in a silicon system with substrate doping in this range). As a result, significant charge can diffuse into and flood a nearby depletion region, shielding electric field lines, and result in a funneling effect. In addition to charge that is initially collected by depletion regions through drift processes, charge which

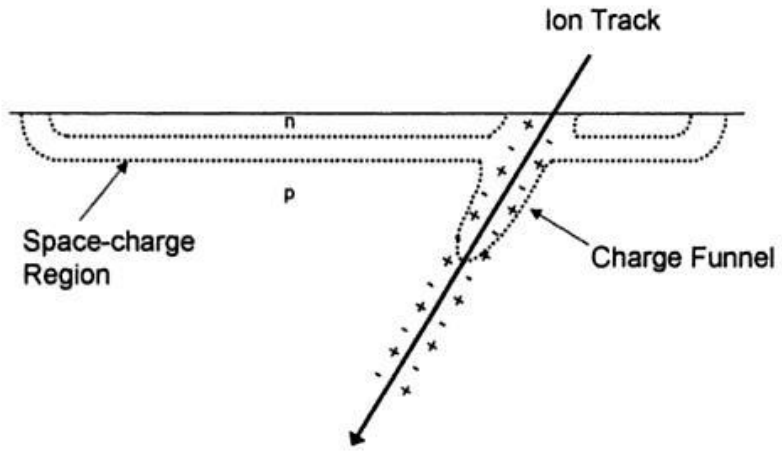

Figure 2.6: Generation of a modulation in the substrate potential and depletion region of a struck junction, resulting in the funneling effect (After [9]).

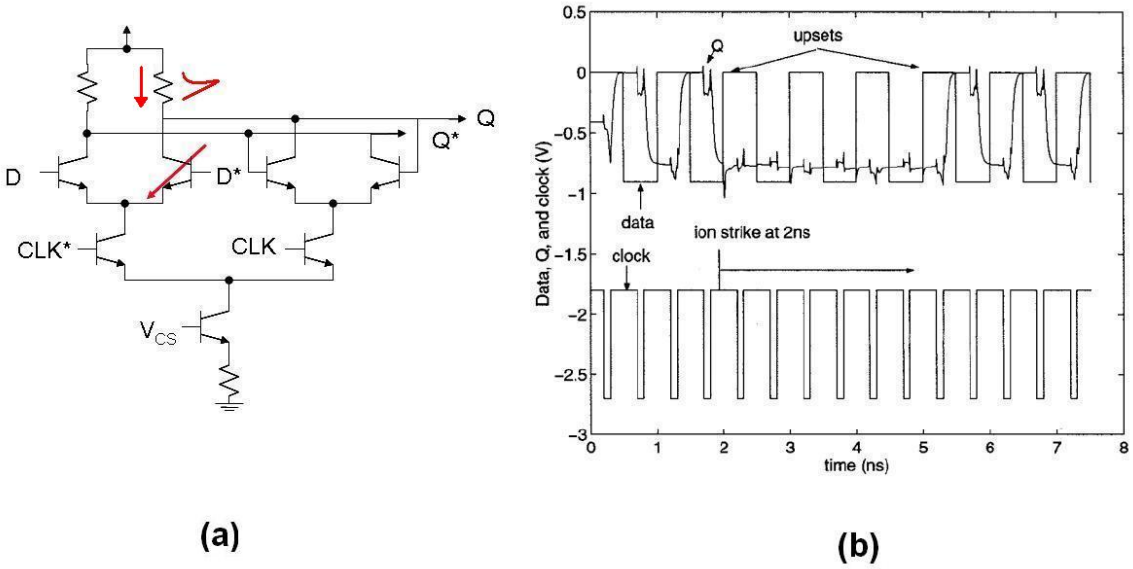

Figure 2.7: A voltage pertubation induced on one collector terminal coupling forward to result in a digital state flip (After [9]).

is generated deep into the substrate can diffuse upwards towards junctions and be collected.

2.3.3 Single/Multiple Bit Upset

As generated charges from ion tracks are collected by the depletion regions of a device, transient currents are induced on the terminals of the device. Given transients of sufficient amplitude and duration, significant voltage perturbations may be introduced as these currents flow through nodal impedances. To understand how this voltage perturbation can result in a single/multiple bit upset, a standard bipolar current-mode logic (CML) digital latch (half of a master/slave topology) is considered. As seen in Figure 2.7 (a), a differential pair controls the direction of current flow through the resistors tied to the collector, while the clocked HBT controls when the input is coupled forward to the output. The positive feedback maintains the previous output of the latch while the input and output are decoupled.

If an ion striking an HBT whose base input is D* is considered when the input D

is logic high and input D* is logic low, the following set of events will take place. The charge generated within the HBT will be collected through the processes mentioned earlier (immediate drift/funneling, and slower diffusion) inducing a current on each of the device terminals. The terminal of interest for this latch is the collector, given that the flow of collector current through the resistor controls the output of the latch. The direction of the transient current flow can be determined by recognizing the carrier type collected at the terminal interior to the device. For NPN transistors (predominant in SiGe BiCMOS platforms due to their inherently higher speeds), the collector is doped n-type, resulting in generated electrons flowing out of the collector corresponding to a current flowing into the collector. If the amplitude of this transient current is sufficiently high, the voltage drop across the resistor will be large enough to correspond to a digital zero (instead of the expected output of a digital one). If this perturbation occurs during a clock edge, the incorrect logic state will be latched into the cell, resulting in an SEU. If the clock is operating at a high enough frequency, the duration of the current pulse may be sufficient to result in multiple bit upsets, as illustrated in (b) of Figure 2.7.

A figure of merit that has arisen to correlate particle strike events with a corresponding SEU rate is the critical charge [30]. If the transient current pulse on a device terminal is integrated over the entire duration of the pulse, a quantity corresponding to the total amount induced charge on the terminal is acquired, as illustrated in Figure 2.8. The integral of the current at which the latch first experiences an upset is defined as the critical charge for the circuit. This variable has been shown to be a highly circuit-specific term whose value and validity strongly depend on the nodal impedances of a device embedded in a circuit [26]. Despite the dependence of critical charge on circuit parameters, understanding charge collection mechanisms of a device and work towards suppression of collection remains fundamental for improving the sensitivity of transistors to SEU.

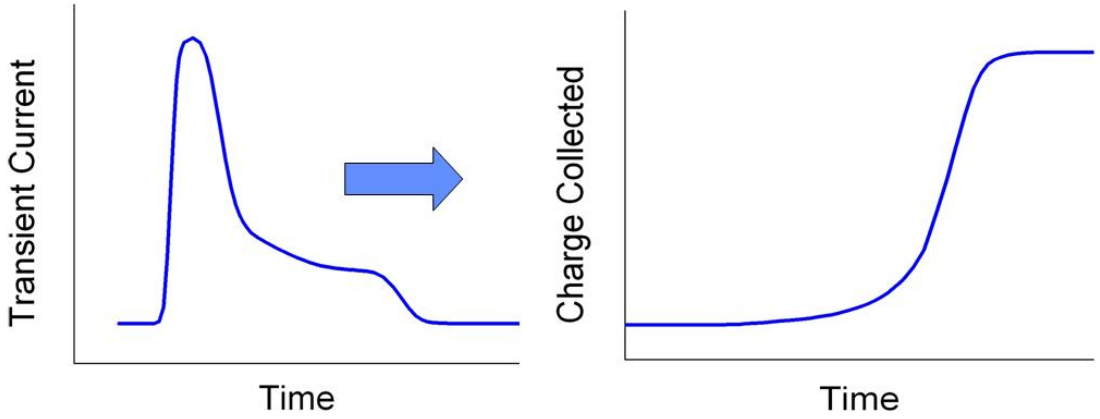

Figure 2.8: Representative integrated charge for a given transient current waveform on a device terminal.

2.4 Literature Review of SEE Mitigation Techniques

Given the susceptibility of SiGe BiCMOS technology to SEE, a large amount of research has been dedicated to address this sensitivity. The mitigation techniques that have been developed fall within two categories radiation hardening by process (RHBP) and radiation hardening by design (RHBD). RHBP techniques are the most costly, and employ modifications to a standard fabrication flow, by either introducing additional mask layers or introducing new materials. Substrate engineering for SEU mitigation is one such RHBP methodology that has been proposed by several groups and examined through both simulation and fabricated structures. One such technique that has been proposed is the incorporation of a highly doped, buried p+ blocking layer beneath the deep trench of bulk SiGe technologies [29]. Given that the substrate is only moderately doped p-type, this highly doped layer will establish opposing electric field lines that will suppress the collection of charges generated in the bulk. This methodology is simulated to be effective for reducing charge collection events by more than 70% for ion strikes outside of the deep trench [29]. A second substrate engineering technique which is commercially available is replacing bulk technology with a silicon-on-insulator technology. With an SOI platform, the volume of the sensitive region is significantly

reduced reducing total charge collection, since the insulating layer blocks charge collection from the substrate [39]. Using SOI technology can be very successful for mitigating single events; however, SOI platforms are much more costly than their bulk counterparts. The cost of a technology is a heavy weighting factor when making selections for space applications; therefore, it is desirable to continue to investigate SEE hardening methodologies in bulk platforms to attain levels of hardness comparable to SOI technologies.

Unlike RHBP techniques, RHBD employs device layout or circuit architecture changes using a commercial foundry's process as is no modifications to existing process of violation of design rules occur [16]. As such, these hardening methodologies are substantially cheaper (no additional processing costs); however, current effective circuit hardening techniques often come with significant area and power penalties. At the present, the most effective hardening practices involve spatial redundancy of digital logic with some form of majority voting. These practices can double (gated cell feedback, GFC) or triple (triple mode redundancy, TMR) the area/power penalties of a given application, as such, it is preferable to explore RHBD techniques on the device level to avoid spatial redundancy of logic blocks. One such device-level RHBD method is the employment of highly doped n+ guard ring structures (termed N-Ring) around a device [35]. These N-Rings are reverse biased, resulting in depletion regions wrapping around the structure that compete with the subcollector-substrate junction for charge collection. The structures are simulated for being most effective at eliminating charge collection events for ion strikes outside the deep trench. There is minimal area and power penalty for incorporating these structures into a circuit. Third generation SiGe HBTs have been designed and fabricated with this N-Ring concept and measurements show no compromise to either dc or ac characteristics. Additionally, ion microbeam data has validated simulation data, showing considerable attenuation of charge collection events occurring for ion strikes outside of the deep

trench. To further harden devices, it is desirable to reduce charge collection events occurring not only outside the deep trench, but also within the deep trench of a device. The two original RHBD techniques that are presented are aimed at accomplishing exactly that, and are described in the following two chapters.

CHAPTER III

IMPACT OF DEEP TRENCH ISOLATION ON SEU EVENTS

3.1 Introduction

In this chapter, a new approach for mitigating charge collection events corresponding to ion strikes within the active area of a device, by reducing the depth or completely removing the deep trench isolation (DTI), is introduced. Although previous studies have identified the repercussions of complex charge collection mechanisms in technologies incorporating deep trench isolation [38], no studies have been performed on the potential mitigation of SEU through the inclusion/exclusion of this processing step. In the first section of this chapter, an overview of deep trench isolation is provided, describing its electrical benefits and suspected effects on SEU. Experimental data on both the total dose tolerance and charge collection statistics of two of IBM's 3rd generation SiGe platforms (having different deep trench depths) are presented and analyzed. This experimental data is then supported with full three dimensional device simulations which explore the evolution of carrier distributions following ion strikes on a device. The chapter is concluded with some insight into possible hardening schemes from the information uncovered through both simulation and experimental studies.

3.2 Advanced Electrical Isolation: Deep Trenches

In the early years of IC fabrication, electrical isolation between transistors on chip was achieved through junction isolation (a reverse biased n+ ring enveloping the device). This isolation tended to have the characteristic of large capacitive parasitics between the device collector and substrate as well as large leakage currents under high

Table 3.1: Improvements to Substrate Parasitic Capacitances using Deep Trench Isolation (After [15]).

Parasitic Capacitance	Si Platform w/o DTI	SiGe Platform w/ DTI
$C_{CS}(Area)$	0.15 $fF/\mu m^2$	0.08 $fF/\mu m^2$
$C_{CS}(Edge)$	0.65 $fF/\mu m^2$	0.10 $fF/\mu m^2$
$C_{CS}(Total)$	25 fF	1.6 fF

temperature conditions. Additionally, junction isolated impeded the progress of very large scale integration (VLSI) technology, since large spacing between devices was required. In order to continue the trend of compacting more devices onto a single wafer, a new isolation technique needed to be developed. By etching into the substrate around the device and subsequently filling these trenches with oxide, devices were able to be packed together closer while at the same time reducing parasitic substrate capacitances as illustrated in Table 3.1 [13].

At a preliminary glance, DTI appears to serve a beneficial role in a single event context. As discussed earlier, with the moderately doped substrates in today's SiGe BiCMOS processes, minority carrier diffusion lengths are relatively high. Charges generated deep in the bulk from an ion-generated track are able to diffuse outwards and upwards to the surface. This can easily result in charges being collected by subcollector-substrate junctions of multiple devices, a process known as charge sharing. With the presence of DTI, a significant amount of substrate shielding is introduced, which prevents charge from easily diffusing into the sensitive junctions. Considering an ion strike within the DTI of a device as shown in the cross-sections of Figure 3.1, the response is more ambiguous and requires investigation.

In this Figure the simulated concentration of ionized free carriers as a result of an ion strike to the center of a device is plotted at two given moments in time; (a) directly following the strike and (b) several microseconds after the ion strike. As can be seen, the charge track spreads radially outward to establish equilibrium as well as being collected by the subcollector-substrate junction. It appears as if the DTI is impeding

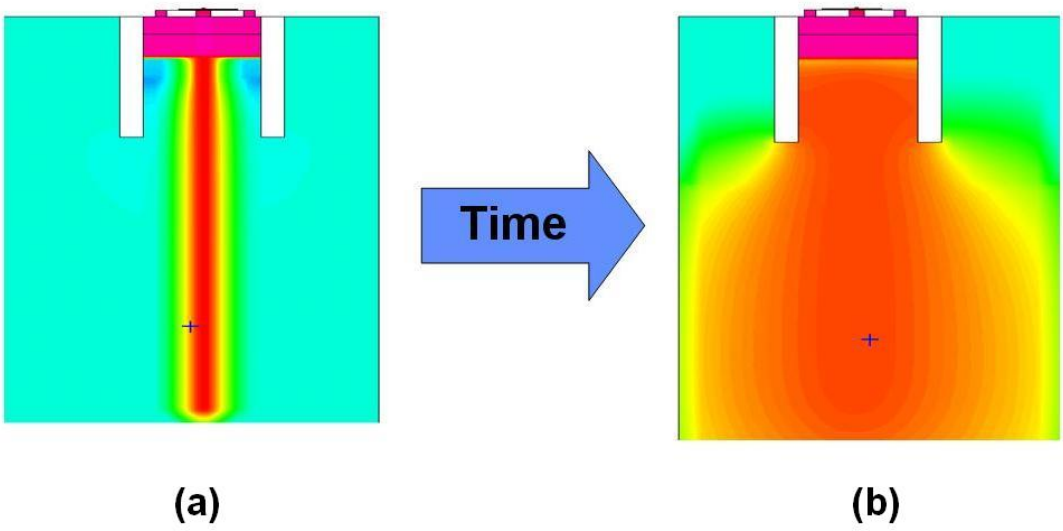

Figure 3.1: Progression of deposited charge due to an ion strike at times (a) directly after the strike and (b) several microseconds later.

carrier diffusion in the vicinity of the sensitive junction, confining the carriers near the depletion region where they will be collected. This raises the question of whether shallower, or no DTI would promote more radial diffusion away from the device's sensitive junction, thereby reducing charge collection. To answer this question, devices from two different 3rd generation IBM platforms (having different deep trench depths) were tested in a microbeam environment to quantify their charge collection statistics.

3.3 Device Technologies

IBM's 3rd generation platforms are exemplary technologies for incorporation in satellite communication systems given their aggressive scaling and innovative device topology which leads to extended ac performance while maintaining acceptable breakdown levels. The two platforms used for this study were the 8HP platform [14] (a high performance platform) and the 8WL platform [18] (a cost-effective platform with moderate performance). To distinguish between the two platforms, from here on the 8HP technology will be referred to as the high-performance (HP) platform and the 8WL technology will be referred to as the cost-performance (CP) platform. Both

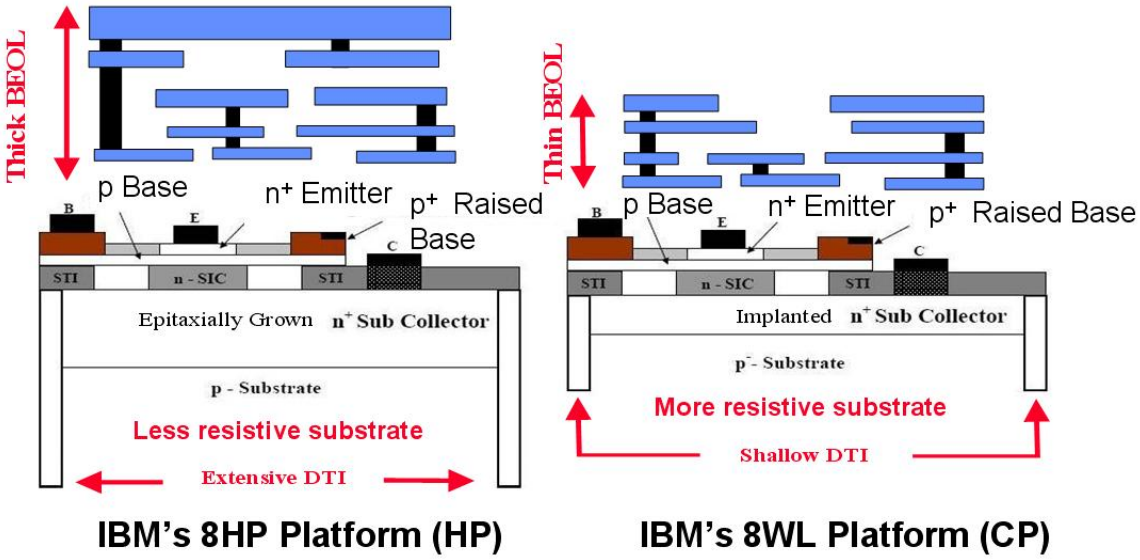

Figure 3.2: Sample device cross sections for both the HP platform (a) as well as the CP platform (b) are shown, with important process variations, in the context of radiation effects, highlighted.

platforms are a 130 nm technology node that share many similar processing steps characteristic of standard high-speed SiGe HBTs. These include a raised-extrinsic base, a retrograded collector, and shallow trench isolation schemes. A cross section of the two platforms is shown in Figure 3.2. The important difference between the two platforms, conducive to the experiment at hand, is the depth of the deep trench isolation step. The HP platform uses a trench depth of approximately eight microns while the CP platform uses a trench of only approximately three microns. There are several other differences between the two platforms which need to be accounted for, as they will have an effect on the experiment. These differences include a more resistive substrate, an implanted sub-collector (CP) as opposed to an epitaxially grown sub-collector (HP), different collector reach-through processes, and different back end-of-the-line thicknesses. All of these differences lead to the lower cost of the CP platform.

3.4 Experiment Details

To understand the affects of DTI depth on the SEU susceptibility of the two platforms, charge collection statistics were measured using an ion microprobing technique. Identically sized transistors from both the HP and CP deck were irradiated with an ion microbeam, allowing knowledge of the spatial location of the ion strike for a given set of charge collection measurements on the device terminals. Using this microbeam data, device decks were constructed in a full 3-D TCAD software package, allowing ion strike simulations to be executed and the physics of charge collection mechanisms to be uncovered. Additionally, to verify that changes in the DTI have no affect on total dose response, both 63 MeV proton irradiation and 10 keV X-ray irradiation were performed. Given that the depth or presence of the DTI has no impact on the thicknesses of the sensitive oxides of a SiGe HBT (emitter-base spacer and STI), no difference between the TID responses of the two platforms is expected.

3.4.1 Total Ionizing Dose Testing

SiGe HBTs of matching emitter areas ($A_E = 0.48\mu m^2$) were used for a one-to-one comparison of the damage response between the HP and CP SiGe HBTs to TID. All transistors were packaged in 28 pin dual-inline packages (DIPs) with all transistor terminal wirebonded out to package pins and independently irradiated with 63 MeV protons and 10 keV X-rays. This facilitated easy in-situ measurements and allows for various bias configurations during irradiation. All device terminals were grounded during both irradiations, a bias which has been shown to be a worst-case scenario for transistor damage. The 63 MeV proton irradiation was performed at Crocker Nuclear Laboratory at the University of California at Davis, whose set-up can be found in [20]. A dose rate of 1 krad/second was used, with particle fluences ranging from 1.19×10^{12} p/cm^2 to 1.49×10^{13} p/cm^2. The equivalent gamma dose points (all units in SiO_2) of 300 krad, 600 krad, 1 Mrad, 2 Mrad, and 3 Mrad were achieved. Previous TID work

in SiGe platforms has shown no evidence of any low-dose rate (ELDR) effects, so no low-dose rate experiments were performed [36]. The 10 keV X-ray irradiation was performed at Vanderbilt University's faciling with an ARACOR X-ray test system. A dose rate of 1 krad/s was employed to achieve doses of 180 krad, 540 krad, 1080 krad, 1800 krad, and 5.4 Mrad. Pre- and post-irradiation dc characterization of the response to both radiation sources consisted of forward Gummel measurements taken at a collector-base (V_{CB}) voltage of 0 V. The excess base current density (extracted at a base-emitter bias, V_{BE}, of 0.6 V) was used as the figure-of-merit for characterizing the total dose degradation of both platforms.

3.4.2 Ion Microprobe Testing

For the charge collection studies performed, a high spatial precision (1 μm x 0.5 μm resolution) heavy ion microbeam at Sandia National Laboratory's Microprobe facility was utilized. Ion beam induced charge collection (IBICC) measurements on both HP and CP SiGe HBTs with identical areas ($A_E = 0.36\ \mu m^2$) and a C-B-E-B-C layout were performed. All four transistor terminals (base, collector, emitter, and substrate) were monitored simultaneously, with total integrated charge and accompanying X-Y position information recorded for each ion strike event. The experiments were conducted using normally incident 36 MeV ^{16}O ions, having a surface incident linear energy transfer (LET) of 5.4 $\frac{MeVcm^2}{mg}$ and a range of 25.5 μm in silicon, as determined by the Stopping and Range of Ions in Matter (SRIM) calculations [40]. Samples were prepared in 28 DIP packages with all terminals grounded except for the substrate which was held at -4 V. These biases were intended to mimic transistor off-state conditions, a highly sensitive region of operation for SEU. No etching was performed prior to beam exposure, so any ion energy lost in the overlayers of the devices had to be estimated using SRIM calculations.

3.5 Measured Results

3.5.1 TID Results

The base current degradation of SiGe HBTs due to ionizing radiation has become a well-understood phenomenon and has been documented for numerous technology generations, industry platforms, and radiation sources [36, 37]. Radiation-induced holes within oxides migrate to semiconductor-oxide interfaces, breaking silicon-oxygen bonds and creating generation-recombination traps that induce larger base currents. The sensitive interfaces present in SiGe HBTs are specifically the emitter-base (EB) spacer oxide for forward-mode degradation and shallow trench isolation (STI) oxide for inverse-mode degradation. Based on this understanding of damage sources, it has been predicted that changes in the depth of the DTI should have no effect on the TID degradation of SiGe HBTs.

Given the predominance of forward-mode operation for circuit architectures, the measured results will only focus on this regime. Given the limited supply of hardware available for all experiments, only single device statistics are available for each radiation source. Although still valuable for comparison purposes, it should be understood that with the probabilistic nature of radiation interactions, these specific values are not representative for every device in the given technology. The excess base current density (ΔJ_B) as a function of absorbed dose for both the CP and HP devices, irradiated with 63 MeV protons and 10 keV X-rays and extracted at a bias value of $V_{BE} = 0.6$ V, is depicted in Figure 3.3. Several trends are evident in this figure which will highlight some of the differences between the two technologies.

A trend in accelerated damage of devices for X-ray radiation is seen in these data sets, as has been noted in [37]. This increase in sensitivity to X-rays can be attributed to the higher charge yield (more un-recombined holes free to migrate to the oxide-semiconductor interface) as compared to 63 MeV protons [28]. Although classically these radiation sources have been shown to have comparative damaging

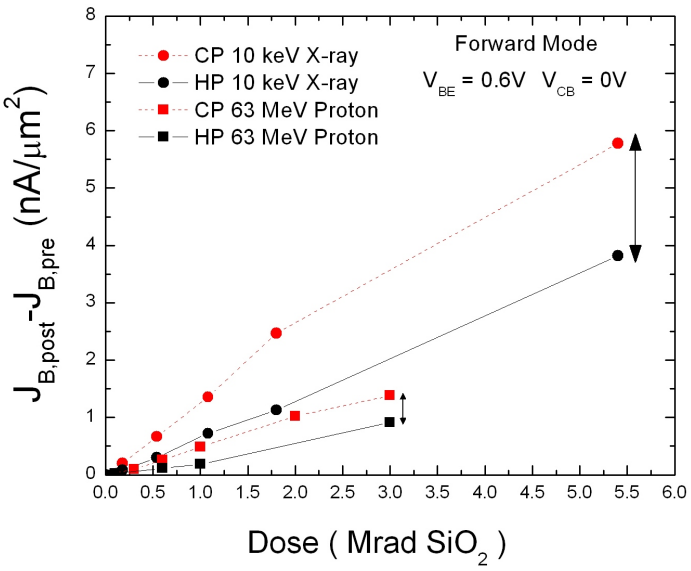

Figure 3.3: Excess base current of identical area ($0.12\mu m \times 3\mu m$) devices from the CP and HP platforms, extracted at a V_{BE} of 0.6 V and a V_{CB} of 0.0 V, for both 63 MeV proton and 10 keV X-ray irradiations.

properties, these studies have centered on MOSFET devices where electric field lines are well defined. For bipolar devices, the field lines in spacer oxides are fringing and not uniform as are E-fields within the gate oxides of MOSFETs.

Both data sets indicate that the CP device is inherently softer to TID as compared to the HP device. Given the lack of dependence of the deep trench on base current kinetics, this exaggeration of excess base current can be attributed to either an increase in the overlap of the EB spacer for the CP technology, or variations in the composition of the oxide structure. However, it should be stressed that despite the observation that the CP platform is softer; at typical bias levels to acquire peak f_T ($V_{BE} \approx 0.85$ V) no gain degradation is experienced in either the CP or HP platforms.

3.5.2 Heavy Ion Microbeam Results

IBICC measurements provide three dimensional integrated charge induction profiles for all device terminals. However, given that current-mode digital bipolar logic (CML) typically employs the collector node of the transistor as the output node of the circuit,

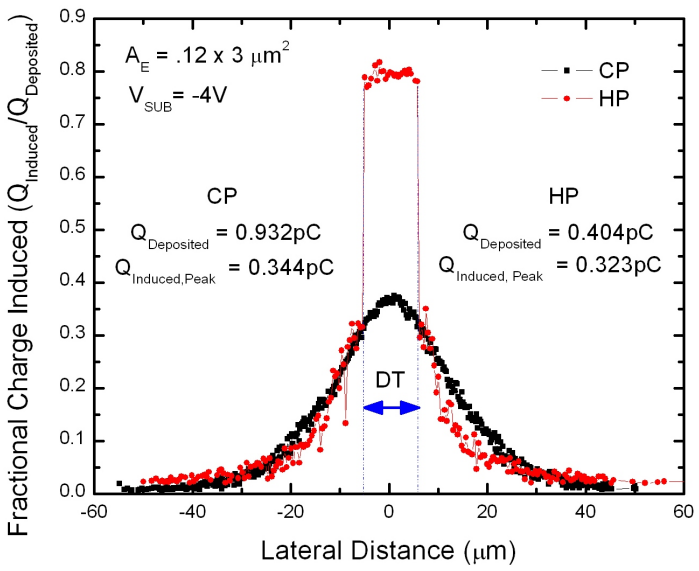

Figure 3.4: A 2-D cut through the collection peak of the measured fractional collector-collected charge for both the CP and HP devices. Separate charge depositions for the two platforms (due to the substantial BEOL thickness differences) are also indicated, in addition to the peak collection value.

we focus on the collector-induced charge following an ion strike. Figure 3.4 shows 2-D cuts through the center of the devices of the 3-D collector-induced charge data sets (Z direction collapsed onto the X-Y plane with one coordinate held constant) obtained for both the CP and HP SiGe HBTs. The data has been plotted in the form of a fractional charge induced ($Q_{induced}/Q_{deposited}$) since ion energy loss in the overlayers of the devices are not equivalent, implying different amounts of charge deposited in the two platforms. To understand the difference in deposited energy between the two platforms, one must reference the cross-sections of the two platforms. As mentioned previously, the HP platform has a distinctly larger BEOL process due to both increased metal layers and thicker metal layers as compared to the CP platform. Back calculating the energy lost of the oxygen ion in these overlayers using SRIM, we find that there are significant differences in the energy of the oxygen ion penetrating the surface of each device. These differences in energy will correspond to two distinct LETs for the ions striking the two platforms hence two separate amounts of deposited

charge. For the CP platform, the 36 MeV oxygen ion is attenuated to 29 MeV, or a corresponding LET of 5.69 $\frac{MeVcm^2}{mg}$, while for the HP platform the oxygen ion is attenuated to 9 MeV, or an LET of 6.93 $\frac{MeVcm^2}{mg}$. The theoretical charge deposited, calculated from the ion LET and penetration depth, is 0.932 pC and 0.404 pC for the CP and HP platforms respectively.

By plotting the fractional induced charge, the response to an ion strike is normalized, and the two platforms can be directly compared. There are several striking characteristics to be noted from Figure 3.4, the first being that the shallower trench isolation ($\approx 3\mu m$ for CP as opposed to $\approx 8\mu m$ for HP) of the CP device leads to an increase in collected charge outside of the subcollector-substrate junction (defined by the boundaries of the trench isolation). As opposed to the sharp drop in induced charge for HP devices due to deep trench isolation (trench boundaries indicated by arrows in Figure 3.4), deposited charges in the CP device outside of the active area can freely diffuse towards the subcollector-substrate junction and be collected. This gradual, smooth decrease of induced charge on the collector terminal moving outwards from the active area of the CP device implies a wider range of sensitive area for upsets when compared to the HP device.

3.6 3-D TCAD Simulations of DTI Depth Dependence

3.6.1 HP platform versus CP Platform

Full 3-D models of devices from both platforms were built using Computational Fluid Dynamics Research Corporation's (CFDRC) finite element modeling software package NanoTCAD. The decks were calibrated to both measured dc characteristics, as well as microbeam data an iterative process involving adjustment of minority carrier lifetime model parameters within various semiconductor regions. NanoTCAD ion strike simulations employ a Gaussian charge generation with a peak time of 2 picoseconds. An ion LET of 5.4 $\frac{MeVcm^2}{mg}$ was used for both platforms for a direct

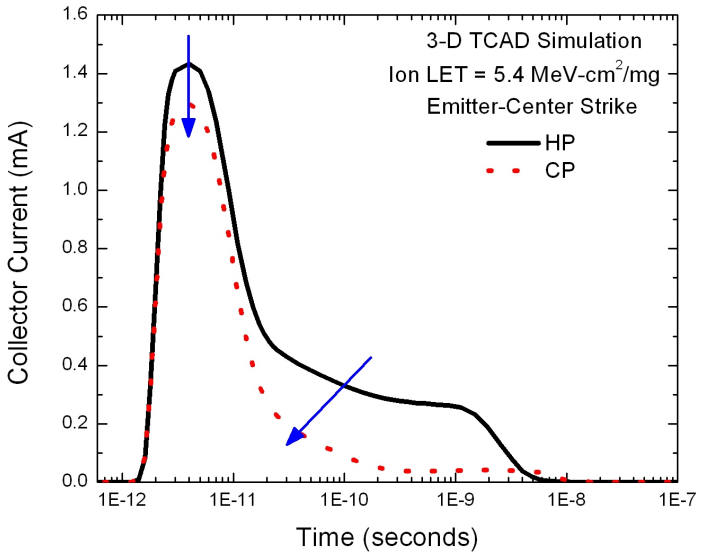

Figure 3.5: Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 $\frac{MeVcm^2}{mg}$. Reductions to peak current and significant mitigations of "tail" currents are evident for the CP device.

comparison of the charge collection mechanisms inherent to each platform. The spatial location for the ion strike was initially chosen to be the center of the emitter for both the CP and the HP device. This position has been determined to be the most sensitive strike coordinate, resulting in an ion passing through all junctions of the device. Figure 3.5 shows the current transient waveforms acquired from the simulation of a normally incident ion strike on the center of the emitter of both devices. These waveforms retain a similar shape between the two platforms; a shape that has been attributed to quick collection of charges from modulated electric fields in the substrate (the classic funnel effect), coupled with drift-diffusion collection of generated carriers [11, 12, 22, 10]. There is significant attenuation of the slow tail collection (20 ps 20 ns) in addition to a lower, maximum peak current spike in the transient for the CP platform when compared to the HP platform. This current reduction couples to a reduction in the total integrated charge which is induced on the collector terminal, as seen in Figure 3.6. While the simulated charge collection of the HP platform due to an ion strike with an LET of 5.4 $\frac{MeVcm^2}{mg}$ is approximately 0.8 pC, the CP

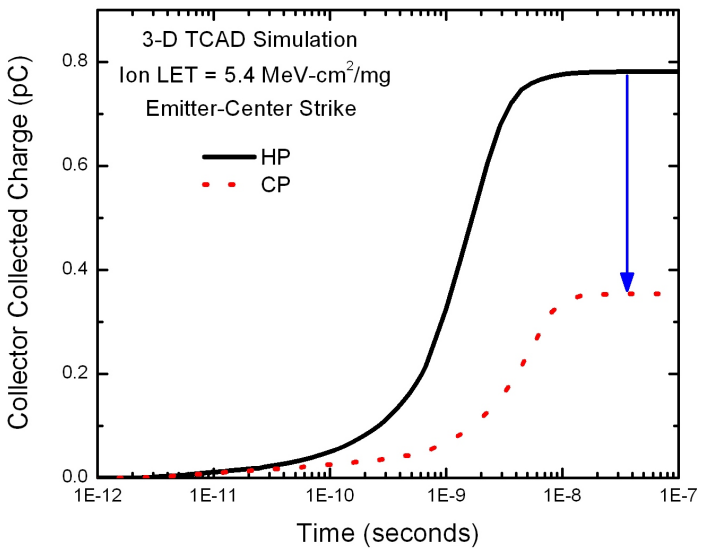

Figure 3.6: Integrated collector-collected charge for simulated emitter-center ion strikes to identical area ($0.12\mu m \times 3\mu m$) CP and HP SiGe HBTs. A near 50% reduction in collected charge is observed for the CP device.

platform only collects approximately 0.35 pC for an ion with equivalent LET. This is a substantial decrease in the charge collected at the collector terminal, and to understand the large difference between these two charge collection profiles, the time evolution of the drift and diffusion current components of the generated charge is examined. These current profiles are taken along a 2-D cut at specific z-locations (depth of the device). Figure 3.7 and Figure 3.8 show the time evolution of the electron drift current density projected on the X-Y plane with one spatial coordinate held constant for both technology platforms. The location of the Z-cut was identical for both the CP and HP platforms and was located directly below the bottom of the deep trench of the HP device. The drift component is observed to be consistently higher for the HP device, stemming from larger field perturbations in the substrate which accelerate electrons in the charge track up into the subcollector-substrate depletion region. Although the CP device also shows a large drift contribution early after the strike (2 ps), the term is smaller than in the HP case, and very quickly shrinks in magnitude. This smaller drift contribution is attributed to the CP platform's lower

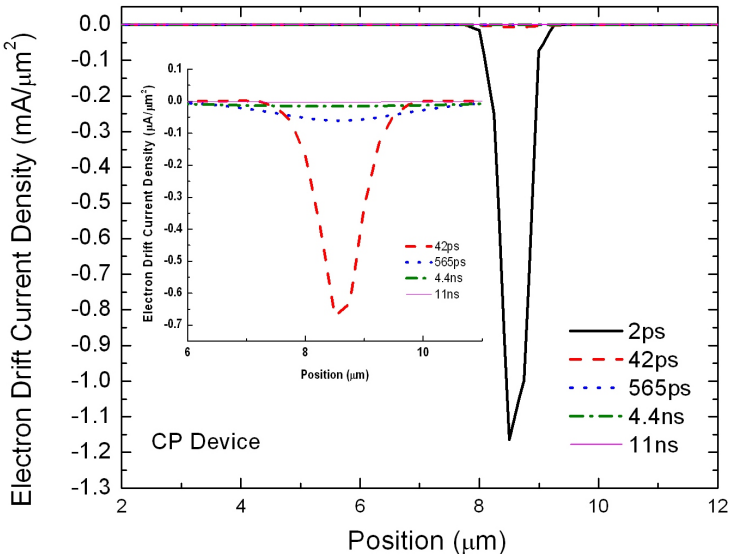

Figure 3.7: Time evolution of the electron drift current density of the CP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current density ($\mu A/\mu m^2$) for times well beyond 2 ps. The electron drift component quickly falls off to extremely low values after only 42 ps following the strike.

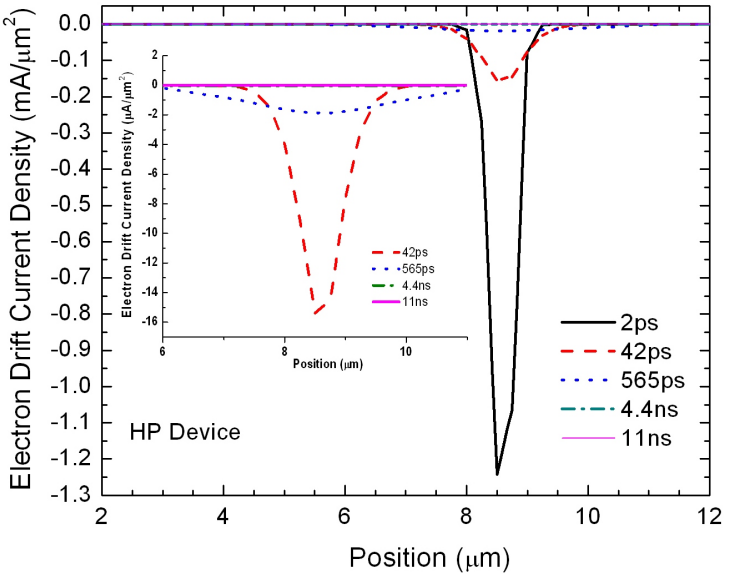

Figure 3.8: Time evolution of the electron drift current density of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current density ($\mu A/\mu m^2$) for times well beyond 2 ps. The electron drift component maintains distinctly non-zero values for nealy a nanosecond after the strike.

peak transient collector current. To understand the origin of this smaller drift current, it is hypothesized that the presence of the deep trenches in the HP platform impedes carrier diffusion away from the sensitive junction; confining free carrier within the trench boundaries and resulting in them being collected across the depletion region. To verify this claim, the diffusion of the carrier concentration over time was analyzed for both simulated device decks.

To understand the rapid drop in the electron drift current component in the CP device, the projection of the time evolution of the radial distribution of generated charge carriers on the X-Y plane is plotted in Figure 3.9 and Figure 3.10, for the CP and HP platforms, respectively. The location of the Z-cut was once again identical for the two platforms and was located directly below the bottom on the deep trench of the HP device. The data from these simulations support our earlier hypothesis that the presence of deep trenches impedes the radial dispersion of free carriers (even below the deep trench!) causing elevated charge collection values. Immediately following the strike, both platforms have nearly the exact same carrier concentration distribution within the charge track. Given that the peak carrier density in the charge track remains roughly constant between the two platforms, yet drift currents are not equivalent, larger carrier diffusion components are expected to be noticeable in the CP device. Increased radial diffusion of free charges is evident in the CP device, with smooth reductions in the peak as carriers spread outward into the quasi-neutral substrate. Referring to Figure 3.10, the HP device clearly shows slower radial diffusion of charge carriers, even for charges below the deep trench implying a coupling effect between charges confined within the DTI, to the charges in the track below the DTI. Significant difference between the diffusion of the two platforms is especially noticeable for a time of 565 ps after the ion strike. Although the peak carrier concentration remains relatively similar between the two devices at this time, distributions spreading from the peak are quite different. Given that charge deposition is identical between

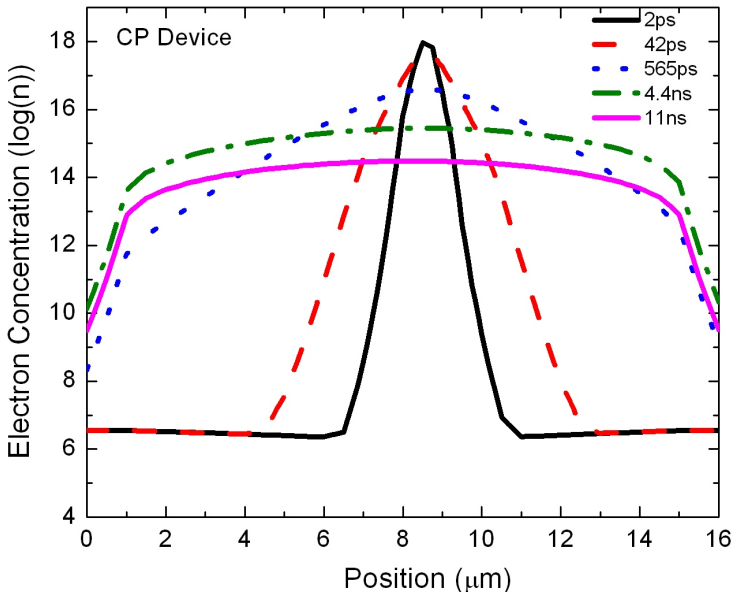

Figure 3.9: Time evolution of the radial diffusion of the carrier concentration of the CP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Large diffusion is evident with smooth spreading of the peak spatially outward in both directions.

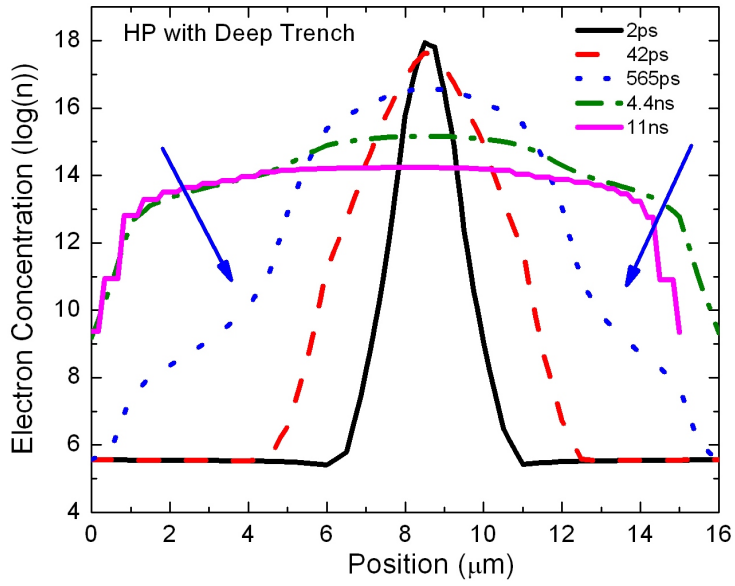

Figure 3.10: Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Significant variation in diffusion between the CP is evident for tims greater than 565 ps.

the two platforms and there is a similar peak concentration for both devices, the charge that has not diffused in the HP device has drifted to the sensitive junction and been collected. With limited differences between technologies, the factors which could impact the charge collection process for the two platforms are the substrate resistivity and the DTI. Previous substrate resistivity studies have shown that higher resistive substrates should suffer from larger charge collection events [26] (in contrast to the measured data and simulations performed herein); therefore, we attribute the decreased sensitivity of the CP device to variations in the depth of the trench isolation structure. To verify this claim, a new device deck was constructed, using the HP deck with the one exception that the deep trenches were completely removed. The same sets of simulations were performed on this deck, and the analysis is presented in the next section.

3.6.2 No DTI Ion Strikes

For a direct comparison of trench dependence on charge collection events, an additional TCAD model deck was constructed using the model parameters from the HP device. This variant incorporated all of the features of the HP platform, except complete elimination of the DTI. No variation in substrate resistivity was made between these two model decks. An ion LET of 5.4 $\frac{MeVcm^2}{mg}$ was used for all strike simulations. A plot of the current transient waveforms acquired from the simulation of a normally incident ion strike on the center of the emitter of both the DTI and no-DTI device is shown in Figure 3.11.

Strong similarities between these results and those for the CP/HP comparison are evident; namely a reduction in peak transient current as well as attenuation of the current tail which couples to a reduction in total charge collected. Examination of the time duration of electric field lines penetrating into the substrate show an equivalent period of charge funneling (which is expected given the identical substrate resistivity);

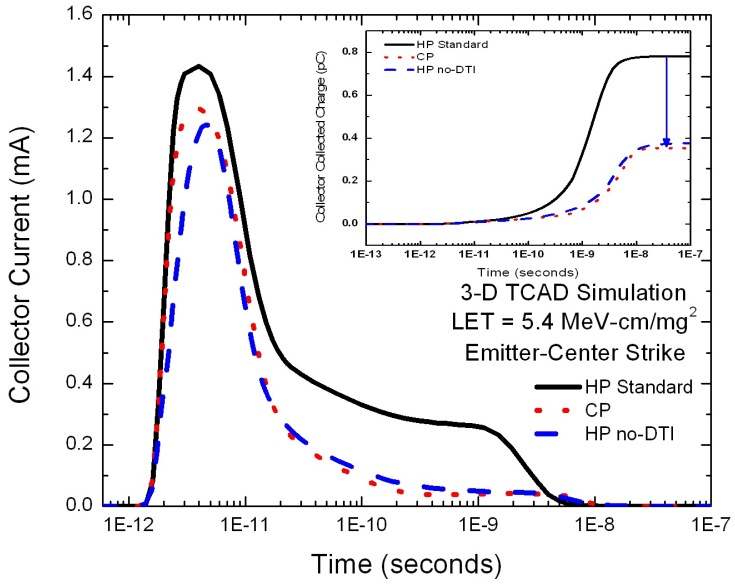

Figure 3.11: Induced collector current transients plotted for all three device decks. Very similar behavior observed between the HP with no DTI deck and the CP deck.

however, smaller electron drift currents exist for the no-DTI device. Once again this reduction can be attributed to larger radial diffusion of charge carriers from the charge track. The projection of the time evolution of carrier density on the X-Y plane is plotted at a depth corresponding to the bottom of the deep trench in DTI device in Figure 3.10 and Figure 3.12, for the DTI device and the no-DTI device respectively. Similar again to the CP device, the no-DTI structure exhibits faster spreading of free carriers from the center of the charge track, generating large diffusion away from the sensitive junction where charge would be collected. This implies that charge collection differences between the HP and CP platform can be attributed to the depths of the deep trench. For emitter-center strikes, it has been shown that charge collection decreases as the depth of the DTI is minimized, peaking when there is absolutely no trench isolation. Previously we have mentioned that DTI does serve a purpose in shielding ion strike events occurring outside the active area of the device; therefore, it is necessary to analyze the impact of reduced trench depths for these strike locations.

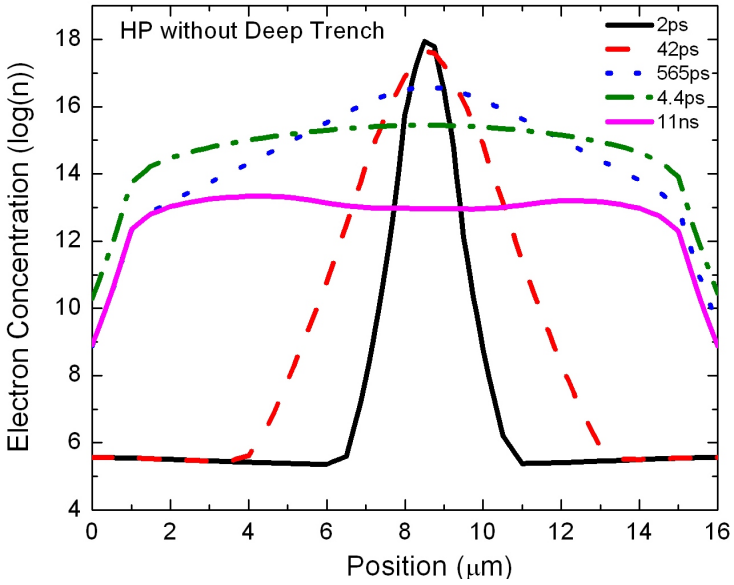

Figure 3.12: Time evolution of the radial diffusion of the carrier concentration of the HP with no DTI device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Similar to the CP platform, much larger diffusion arises when compared to the standard HP device.

3.6.3 Outisde DTI Ion Strikes

Up to this point, only simulated ion strikes orthogonally impingent (i.e. vertical strikes) on the emitter of a device have been under consideration. Despite being the most efficient volume for charge collection events, sensitivity to SEU also exists for ion strikes occurring in the exterior of the trench-enclosed volume, as well as for angled strikes. Recalling the large minority carrier diffusion length of charges in the bulk of SiGe technologies, charges deposited well outside the DTI boundary will have a high probability of diffusing to the active area of the device and be collected before undergoing recombination events. Space is a broadbeam environment, and the exact spatial location of an ion strike can not be predicted; however, comparing the ratio of interior trench area to the area outside DTI, there is a much higher probability for strikes outside the trench. For many SiGe processes, the sensitivity to outside DTI is much less than that for normal emitter-center strikes because of the impedance to carrier diffusion due to deep trench isolation; however, critical charge values for

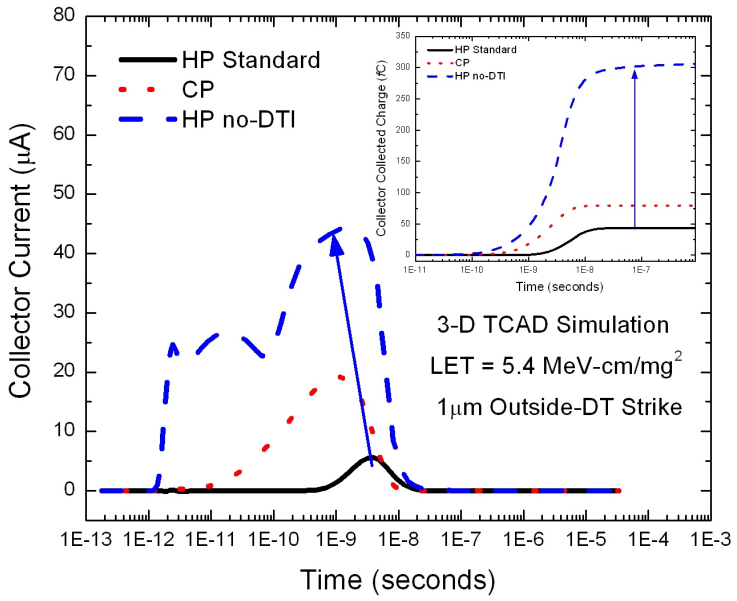

Figure 3.13: Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 $\frac{MeVcm^2}{mg}$ with an inset showing integrated charge collected. Increaes in collected charge for outside DTI strikes are observed for devices with limited DTI and extreme increases are seen in the no-DTI variant due to junction colapse from charges flooding the depletion region.

upset have been found to be as low as 100 fC a quantity which could be collected after outside-DTI strikes for large values of ion LET [33]. For structures which have eliminated or shallower DTI, this sensitivity is greatly enhanced.

The induced collector current transient waveforms as well as integrated charge for the CP device, standard HP device, and no-DTI HP device are shown in Figure 3.13 for an ion with an LET of 5.4 $\frac{MeVcm^2}{mg}$ striking 1 μm from the DTI boundary. Both the CP platform and the HP device with no DTI show greatly enhanced collector current transients, coupling to much larger integrated charges; however, the no-DTI device shows a distinctly different current waveform shape from the other devices. This variation, having much larger currents, is due to the partial collapse of the subcollector-substrate junction from free carriers flooding the depletion region. With no trench isolation impeding the diffusion of carriers to the active area, charges can freely move into the depletion region and compensate the fixed charges present,

collapsing the space charge region. The collapse in the depletion region will result in electric fields being pushed into the substrate to support the applied reverse bias to the subcollector-substrate junction, accelerating charge collection through funneling mechanisms.

A proposed method for almost completely mitigating charge collection outside of the DTI of a SiGe HBT has been previously presented [35]. With the incorporation of a highly doped n+ diffusion layer encompassing the device, a shunt path for minority carrier electrons is introduced, which reduces carrier concentrations reaching the sensitive subcollector-substrate junction. Incorporating these structures into platforms with limited to no DTI (essentially reverting back to a junction isolation platform) will eliminate the caveat of exaggerated charge collection of outside DTI strikes while maintaining reduced collection for ion strikes in the active areas of the device.

3.7 Summary

Through comparisons of IBM's HP and CP technology platforms, the impact of DTI on radiation response has been analyzed in the context of total ionizing dose and single event upset. Although no effect of trench isolation is found to affect the base current degradation resulting from TID, (the accelerated degradation in the CP platform was attributed to differences in oxide thickness and/or compositions, Figure 3.2, a large difference in charge collection statistics is found between the CP and HP devices. To understand these differences, device models were constructed for both platforms, as well as a third device model for the HP device which encompassed no trench isolation, to allow a direct correlation between DTI and SEU susceptibility.

The CP showed substantial reduction in collected charge for emitter-center strikes when compared to the HP device, despite having a lower substrate doping. This decrease in charge collection is attributed to larger radial diffusion of deposited charges away from sensitive depletion regions as well as higher carrier mobility in the bulk

substrate. The incorporation of a deep trench in the HP device impedes carriers from escaping the drift-region of the charge track, resulting in more charge being swept into the subcollector-substrate junction. Although lower doping has traditionally been observed to increase charge collection, these studies have been performed in platforms with identical trench depths. For a device with little to no DTI, the higher carrier mobility accompanying a lower doped substrate will enhance the radial diffusion of charge.

To directly assess the impact of DTI depth, similar simulations were performed on an HP deck with no trench isolation. Similar results to the CP device were observed, namely a drastic decrease in the amount of charge collected. The time evolution of carrier concentration following the strike supports the claim that DTI impedes carrier diffusion away from the sensitive subcollector-substrate junction. Despite the mitigation of charge collection for emitter-center strikes, devices which limit DTI depth show extreme sensitivity to ion strikes outside the active area of the device. Potential mitigation schemes for reducing this sensitivity have been explored previously and suggest that reverting to a reversed-biased junction isolation scheme is preferable over DTI for platforms planned to be incorporated in applications where SEU is a concern. Currently, work is being dedicated to acquire experimental data on charge collection of no-DTI transistors which encompass an N-Ring surrounding the device. Additionally, these structures have been designed within a CML shift register circuit to allow broadbeam testing, compared against standard transistor types.

CHAPTER IV

A NOVEL DEVICE LAYOUT FOR INCREASED SEU MITIGATION

4.1 Introduction

In this chapter, a second device-level RHBD methodology is introduced and analyzed through experimental data as well as through full 3-D TCAD simulations. A new device architecture is proposed, which combines two transistors fabricated together on a shared sub-collector node in a cascoded fashion. This topology decouples the prominent output node of a CML digital device from the highly-sensitive subcollector-substrate junction, while maintaining standard device operational properties. This is achieved by operating the upper device of the cascode topology in inverse mode, which swaps the electrical collector with the physical emitter. Given that there is a shared subcollector (of a standard single transistor size) between the upper and lower device of the cascode, there is zero area penalty for implementing the device.

In the first section, an overview of inverse mode operation is given, including methodologies for optimizing for inverse mode performance. A detailed description of the inverse-mode cascode SiGe HBT is then provided. The total dose response of the device is investigated using a 10 keV X-ray, and the charge collection statistics are analyzed using the heavy ion microprobing technique at Sandia National Laboratory. This experimental data is analyzed and discussed, and the results are reinforced with full 3-D TCAD simulations of the device using CFDRC's NanoTCAD software package.

4.2 Inverse Mode Operation of SiGe HBTs

The inverse mode operation of a device is simply the operation of a bipolar transistor with the emitter and collector terminals swapped into terms of their electrical purpose. This mode of operation suffers from some inherent limitations, which include reductions in both device gain (given the lower doped, single crystal physical collector as compared to the polycrystalline emitter) and maximum operational speed (larger emitter capacitances and base width) when compared to standard forward mode operation. However, with technology scaling the inverse mode performance has also increased, given that doping levels increase with vertical scaling and capacitances shrink with lateral scaling [1]. Recently, the incorporation of inverse mode devices in radiation intensive applications has been investigated [2]. This move is motivated by the potential built-in SEU mitigation of inverse mode operation. When the physical emitter is operated as the electrical collector, the substrate becomes decoupled from the output node (collector terminal in CML logic). The most sensitive junction becomes the electrical emitter (physical subcollector)-substrate junction, which collects the majority of the charge generated in the semiconductor bulk. A significant system speed penalty is paid, however, for incorporating inverse mode devices in a design.

4.3 The Inverse-Mode Cascode SiGe HBT

As described previously, the inverse-mode cascode SiGe HBT is composed of two transistors combined onto a single shared subcollector as depicted in the cross section of Figure 4.1 (a), while the schematic of the structure is shown in (b). This structure is similar to a typical cascoded transistor pair, where transistor Q1 is operated as a common-emitter amplifier while Q2 operates in the unity-current gain, common-base mode. Given sufficient voltage headroom for the device (two VBE drops at minimum), the structure can be operated as a standard single device with an input signal applied to the lower base terminal (Base 1), resulting in amplified current flow through the

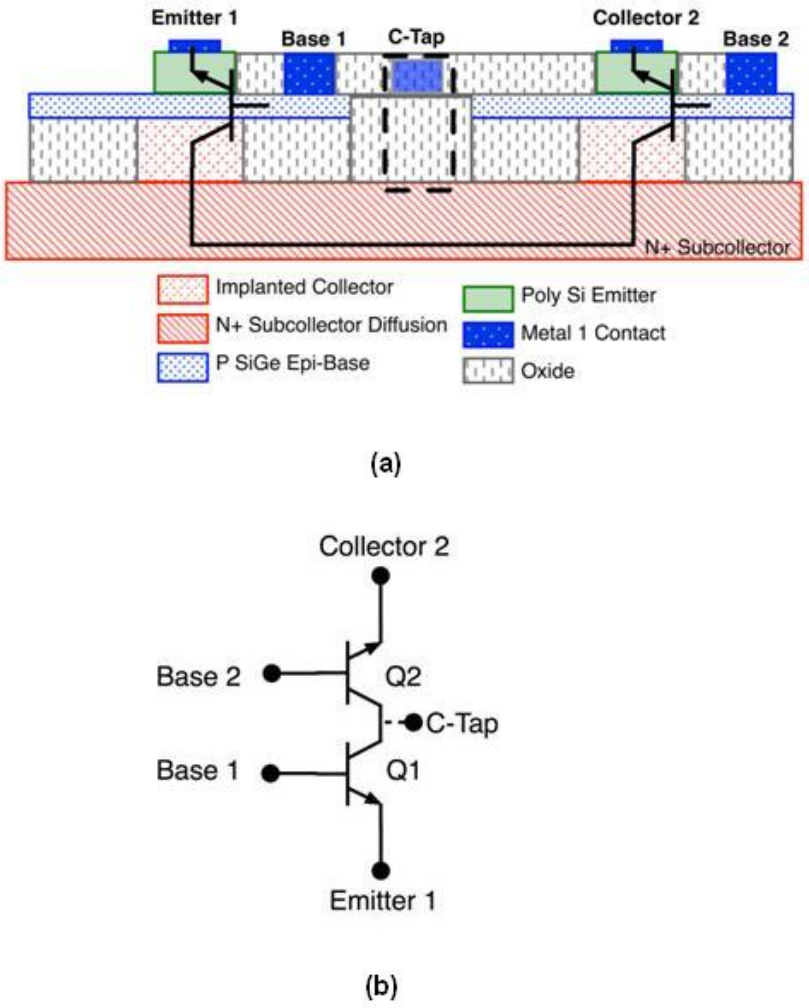

Figure 4.1: A cross section of the inverse-mode cascode device revealing its shared subcollector design is given in (a) while the joint device schematic is given in (b).

collector terminal (Collector 2). To accommodate the shared-subcollector design of our cascode topology, transistor Q2 must be operated in the inverse mode, with the physical collector acting as the electrical emitter and vice-versa. Similar to inverse mode operation of a stand alone device, it is expected that the electrical swapping of the emitter and collector will provide the decoupling of the output terminal and the sensitive subcollector-substrate junction, promoting built-in SEU mitigation. An additional variant of the structure incorporating a contact to the buried subcollector (referred to as the C-Tap terminal) was investigated.

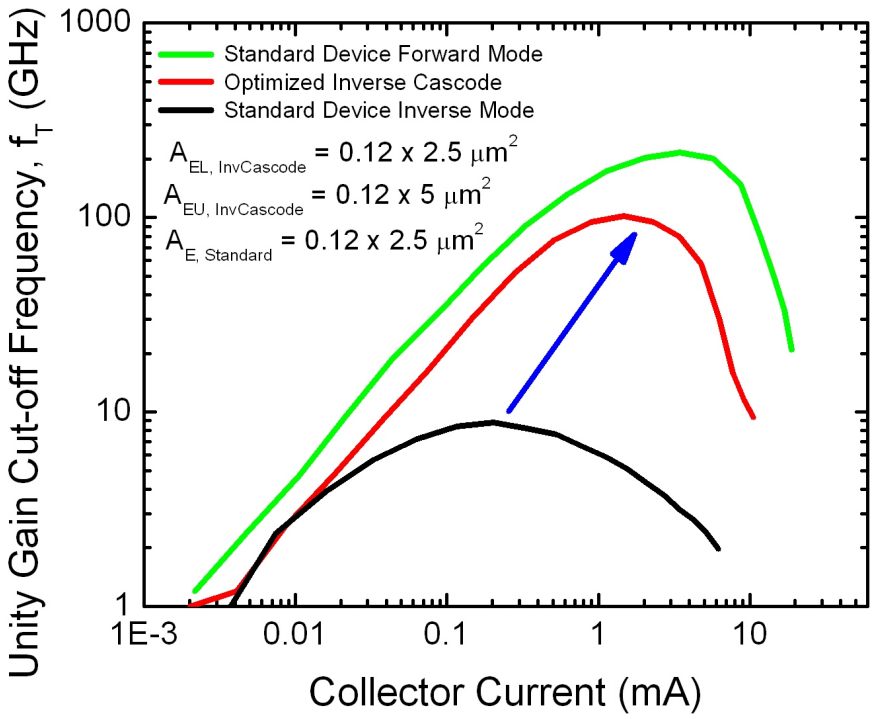

Figure 4.2: Comparison of unity gain cut-off frequency for a standard device, an inverse mode device, and the inverse-mode cascode device.

Although the proposed structure effectively integrates two stand-alone SiGe HBTs, no area penalty exists when comparing the enclosed deep trench area of an inverse-mode cascode SiGe HBT with that of a single stand-alone SiGe HBT in a C-B-E-B-C layout. A slight error penalty exists for inverse-cascode structures where transistor Q2 has been optimized for inverse mode operation (a slight increase in deep trench enclosed area). The optimized inverse-mode cascode device [1], exhibits significantly improved values of f_T as compared to a standard inverse mode device, as seen in Figure 4.2.

Despite an optimized inverse mode device only having a peak f_T of approximately 10 GHz (over an order of magnitude smaller than forward mode operation!) the optimized inverse-mode cascode device has a peak f_T of nearly 100 GHz. This performance was measured on standard SiGe HBTs sized with an emitter area of 0.12 x 2.5 μm^2 and inverse-mode cascode SiGe HBTs with Q1 sized with an emitter area

of 0.12 x 2.5 μm^2 and Q2 sized with a physical emitter area of 0.12 x 5.0 μm^2. With this boost in device speeds, system performances would not have to be sacrificed to obtain mitigation to SEU; however, the SEU susceptibility of these devices still needs to be investigated and is the subject of the next sections.

4.4 Experiment Details

Given that this structure is completely innovative and has not been analyzed in any context, both TID testing and heavy ion microprobing were performed on devices fabricated with this topology in IBM's 3^{rd} generation 8HP technology. The total dose testing was performed at Vanderbilt University using a 10 keV X-Ray ARACOR test bench. Pre and post-irradiation dc measurements were performed so that any degradation in the collector or base currents could be captured. Only a single dose point of 1 Mrad(SiO_2), well above the total sustained dose for typical orbital missions, was captured as a comparison point for pre-radiation measurements. Also, given that only an X-ray source was utilized, no information on displacement damage could be discerned from the data. However, from past experiments it has been shown that displacement damage does not have a significant effect on the standard operation of these 3rd generation SiGe HBTs.

The second set of experiments performed was aimed at quantifying the SEU vulnerability of these new structures. To accomplish this, charge collection statistics of two device variants and different biases were obtained using Sandia National Laboratory's Nuclear Microprobe Facility. Both the standard inverse-mode cascode SiGe HBTs as well as the inverse-mode cascode SiGe HBT with reach-through subcollector contact (C-Tap) were irradiated. A 36 MeV ^{16}O ion beam was used, having a surface incident linear energy transfer (LET) of $\frac{MeVcm^2}{mg}$ and a range of 25.5 μm in silicon. IBICC measurements were performed on all device terminals of the devices irradiated. The standard inverse-mode cascodes were irradiated uner two separate bias schemes: 1)

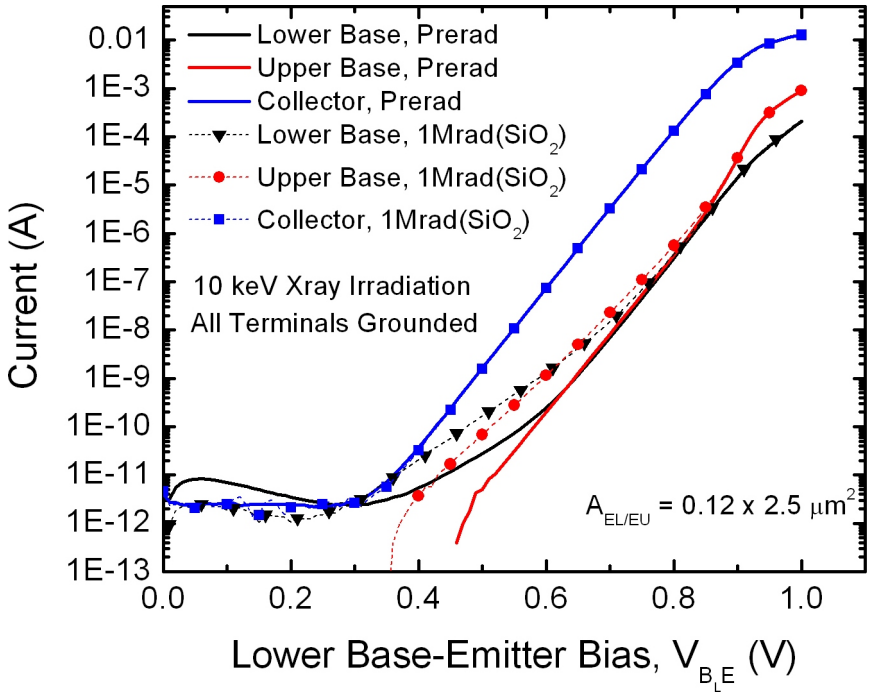

Figure 4.3: TID response of the standard inverse-mode cascode to 10 keV X-rays. Noticeable excess base current is seen at low injection levels, but quickly falls away as biases approach standard "on" biases for circuit applications.

with all terminals grounded except for the substrate held at -4 V, a bias condition allowing direct comparison to previous microprobe data on standard single SiGe HBTs, and 2) 2 V on both the collector and upper base and -4 V on the substrate, with all other terminals grounded. The inverse-mode cascode with C-Tap was irradiated with only a single bias condition, specifically 2 V on the collector, upper base, and C-Tap, -4 V on the substrate, and all other terminals held at ground.

4.5 Experimental Results

4.5.1 TID Results

The forward mode Gummel characteristics of the inverse-mode cascode SiGe HBT measured pre and post 10 keV X-ray radiation is shown in Figure 4.3. The response of this new device shows the same damage characteristics as standard devices in SiGe technologies. The well understood increase in base leakage is evident for both the

upper and lower bases of the inverse-mode cascode. Also, no change in the collector current is measured after exposure to X-rays. The larger excess base current density for the upper base (base of Q2) is attributed to the nature of the mode operation of the SiGe HBT. For inverse mode operation the sensitive oxide interface to radiation damage is the STI oxide. This oxide characteristically has a much larger overlap over the electrical emitter-base junction (physically the collector-base junction), which leads to a greater sensitivity to defect-induced G/R leakage currents [36]. Given that the input signal is applied to the lower base terminal, the gain of the device is measured from the ratio of the lower base current to the collector current. The increase in base leakage of the upper base node is therefore irrelevant for gain calculations. Additionally, nominal on base-emitter biases will be on the order of ≈ 0.85 V, a bias region where no excess base current is evident in the inverse-mode cascode.

4.5.2 Heavy Ion Microprobing Results

The IBICC measurements obtained from heavy ion microprobing revealed very interesting and exciting results. Given that the output of digital CML is the collector terminal, this will be the only terminal where data is reported. The first device presented is the standard inverse-mode cascode SiGe HBT exposed to two different bias configurations described previously. This data is overlayed with charge collection data on the collector of a device using a standard architecture and with a bias scheme of all terminals grounded. A 2-D cut of the integrated charge collection data of the electrical collector terminal (for both biases of the inverse-mode cascode and the standard device), collapsed on the X-Y plane with one coordinate held constant is found in Figure 4.4. There are two important pieces of information to be extracted from this figure. The first is that when the inverse-mode cascode device is irradiated under bias scheme 2, the response overlays with the response to a standard device of equal dimensions. At first this might come at a surprise, given that the output terminal

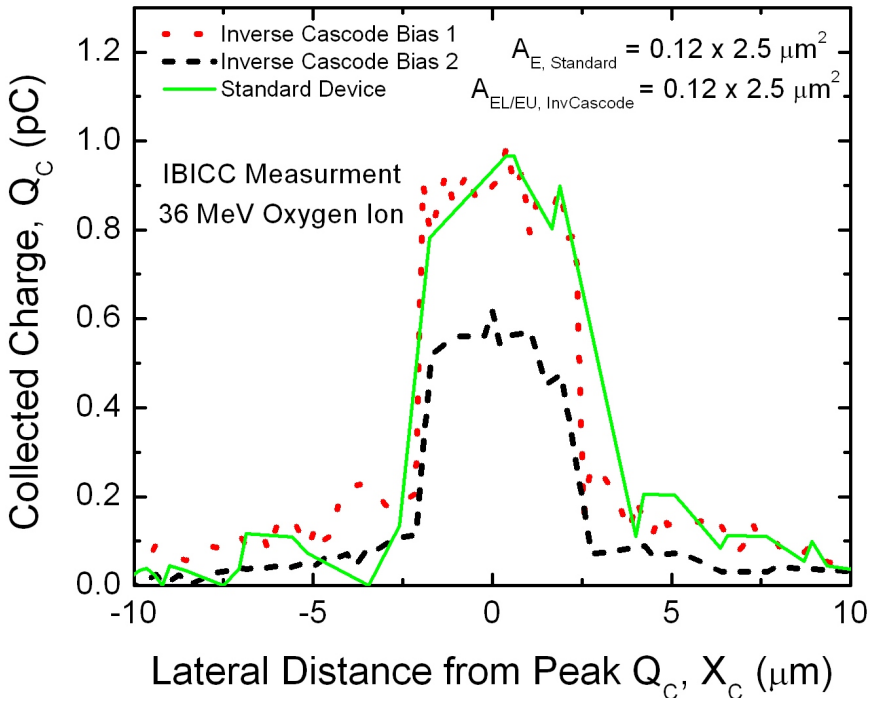

Figure 4.4: Measured 2-D cut of the electrical collector-collected charge data for the inverse-mode cascode subject to two bias schemes, overlayed with standard device charge collection data.

(electrical collector) is isolated from the subcollector-substrate junction, however if we consider the biases applied, we can make sense of the response. For bias scheme 2, electrons that accumulate in the subcollector of the device after being funneled by the subcollector-substrate junction must either recombine in the subcollector, or diffuse into either the upper or lower bases where they will then be collected by either the collector/emitter after drifting across the base-emitter/collector junction. The impedances seen by electrons for traversing these two paths are not equivalent. The energy barrier for majority carrier (electron) diffusion of the upper base-emitter (physical collector) is lower than that of the lower base-emitter junction. This results from the subcollector being forced to 2 V to keep Q2 from turning on (Q1 is biased into an off state, which blocks current flow). This forced potential will reverse bias the lower base-emitter junction since the lower base is being held at 0 V. The bias actively applied to the upper base is 2 V, so the only potential across this depletion

region is the built-in potential of the junction.

The second important fact to glean from this data is that a drastically different response is seen for the bias scheme where all the device terminals are grounded. For this bias, the inverse-mode cascode SiGe HBT shows approximately one-half the total collector-collected charge on the electrical collector terminal when compared to a standard HBT. Once again, understanding the potentials applied and the affect on the energy barriers for free carriers is key to understanding this result. For bias scheme 2, all terminals have 0 V applied to them, so equivalent impedances are seen between the upper subcollector-base junction and the lower subcollector-base junction. It is therefore expected that charge will split evenly between these two paths and be collected equally on the collector and emitter terminals.

The second set of results to be presented and analyzed are the charge collection statistics of the inverse-mode cascode SiGe HBT where the C-Tap is present and biased. These results are shown in Figure 4.5, and are very exciting. For this structure,

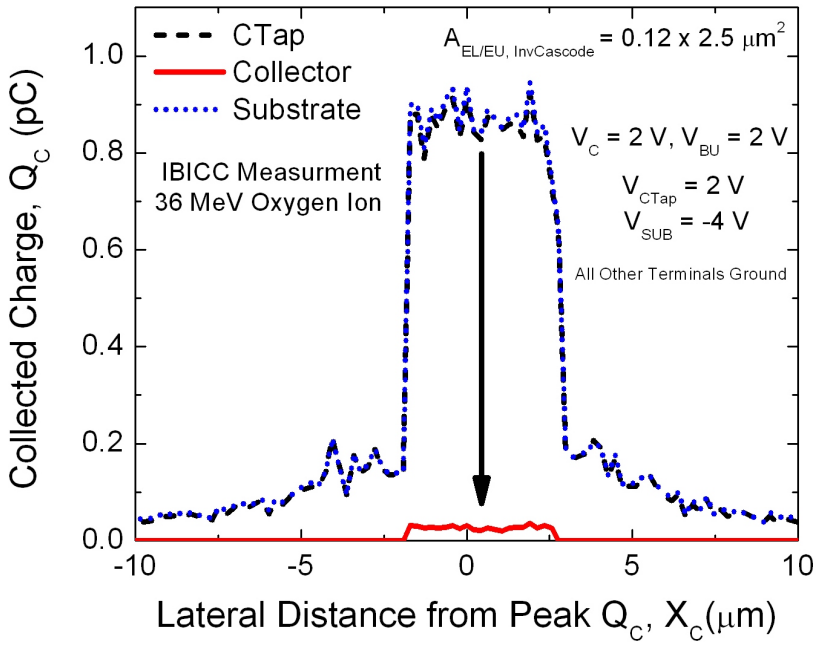

Figure 4.5: Measured 2-D cut of the electrical collector-collected charge data for the inverse-mode cascode with C-Tap showing nearly complete mitigation of charge collection on the electrical collector terminal.

almost complete elimination of charge collection on the electrical collector terminal is displayed. Almost all of the electrons collected by the subcollector-substrate junction are present on the C-Tap terminal, evidenced by the overlying charge collection profiles for the C-Tap and substrate terminals. Unlike the standard inverse-mode SiGe cascode, free electrons which are collected from the substrate-subcollector junction are quickly able to be removed by the C-Tap contact. For the standard devices, charges accumulate in the subcollector, and then diffuse across junctions to be collected be either the emitter or collector terminals.

4.6 3-D TCAD of the Inverse-Mode Cascode SiGe HBT

To validate the experimental results obtained from microbeam testing, the inverse-mode SiGe HBT was built using the calibrated 8HP device deck created from the previous DTI study. CFDRC's NanoTCAD finite element modeling software package was employed to simulate ion strike events on these custom devices. All strike simulations utilized an ion LET of 5.4 $\frac{MeVcm^2}{mg}$ to reflect the LET of the oxygen ions used at Sandia National Laboratory. Strike simulations were executed for the same device types (standard inverse-mode cascode and inverse-mode cascode with C-Tap) and the same biases. Unlike the standard HBT where the most sensitive strike location is the center of the emitter, the most sensitive strike location for the inverse-mode cascode HBT is determined to be the center of the electrical collector (the upper physical emitter), given that an ion will pass through the depletion regions directly tied to the output terminal of the device. These two most-sensitive strike locations for the two different device types are illustrated in the top-down view given in Figure 4.6.

The bias scheme that was simulated under an ion strike condition was bias scheme 1, where the upper base and collector are held at 2 V and the other terminals are held at 0 V (except the substrate which is held at -4 V). The transient current waveforms which are generated on all device terminals is shown in Figure 4.7, and the resulting

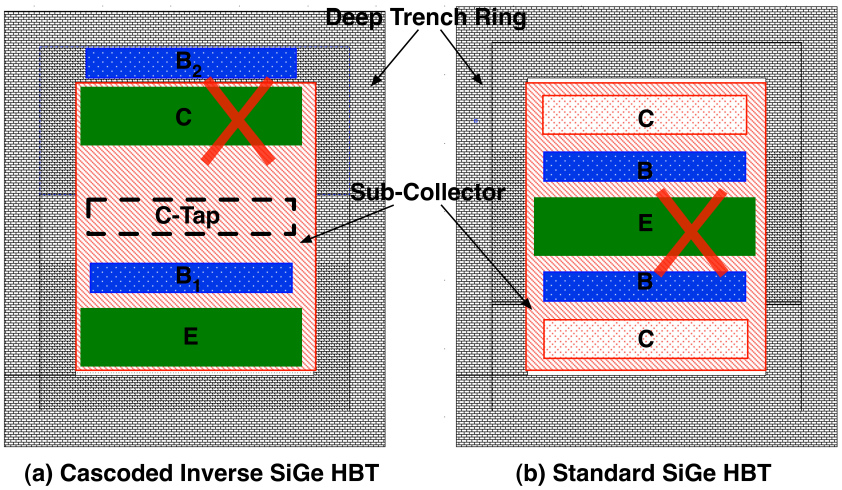

Figure 4.6: Top down comparison of (a) inverse-mode cascode device showing the two variants and (b) a standard device. The most sensitive ion strike locations are shown for each structure with a red "X".

integrated charge profile is displayed in Figure 4.8.

The charge collection profile of the electrical collector terminal resulting from this simulation is in agreement with the experimental data shown previously in Figure 4.4.

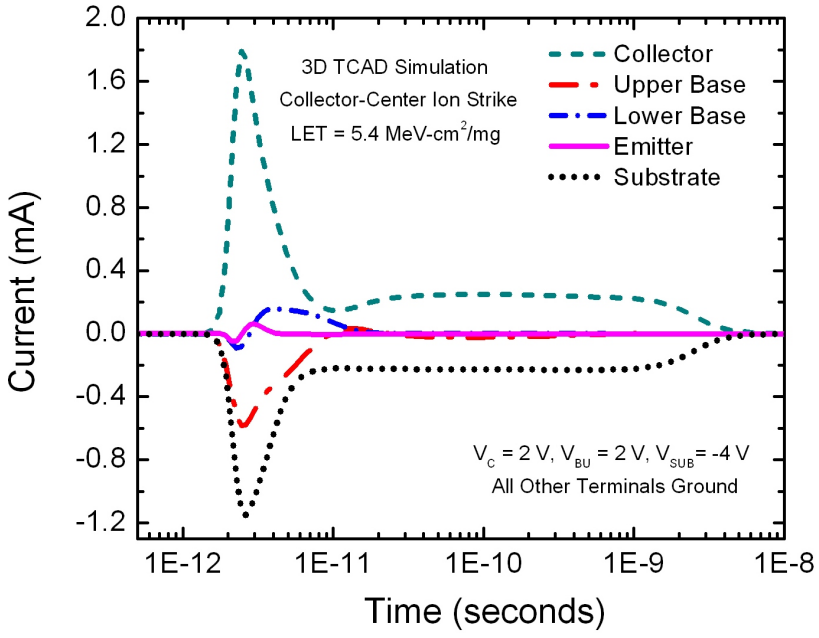

Figure 4.7: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

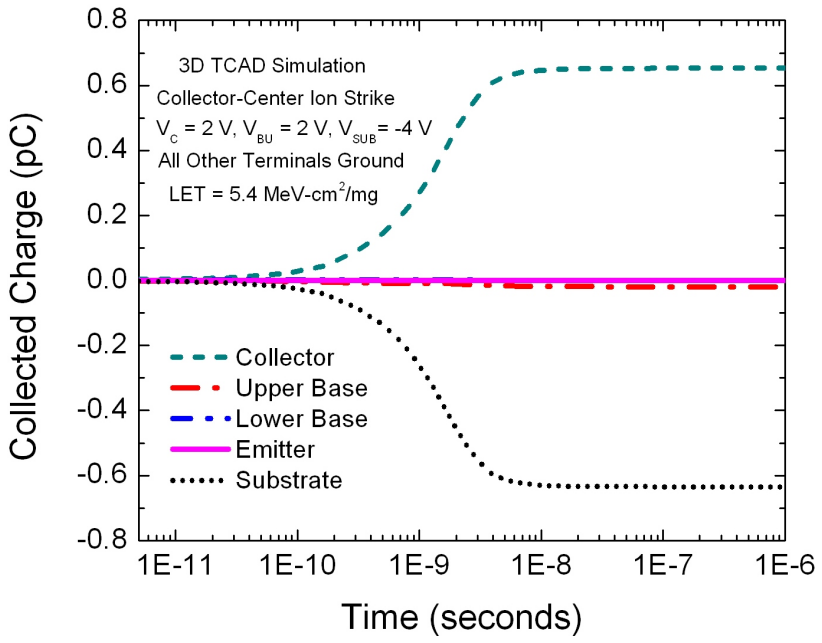

Figure 4.8: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

Nearly all electron charge is collected on the collector terminal, with minimal charge induced on the emitter terminal. Referencing the current waveforms in Figure 4.7, it is obvious that the explanation for this result provided previously is correct. The electrical collector shows two distinct shapes in the transient waveform. These include the current due to the deposition of charge directly within the depletion region of the collector-base substrate (the initial peak), and the current resulting from charge migrating from the subcollector to the collector terminal (the current plateau). Given the smaller impedance to cross the upper base-subcollector junction, the majority of electrons will diffuse across this junction.

The second ion strike simulation that was performed used the same device and strike location, but incorporated bias scheme 1. The simulated output current waveforms for all device terminals is shown in Figure 4.9 and the resulting integrated charge profiles is shown in Figure 4.10.

Once again, excellent agreement between experimental data and simulation data is

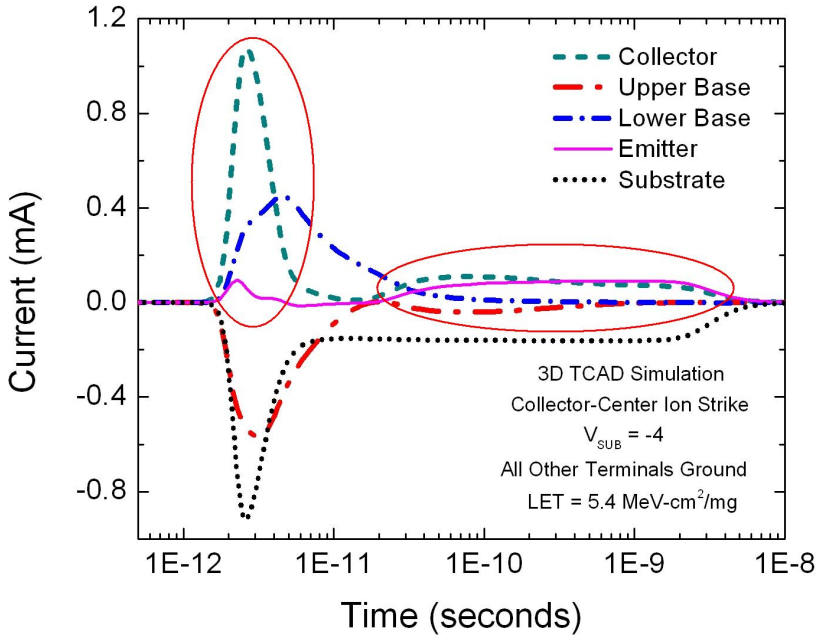

Figure 4.9: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 1.

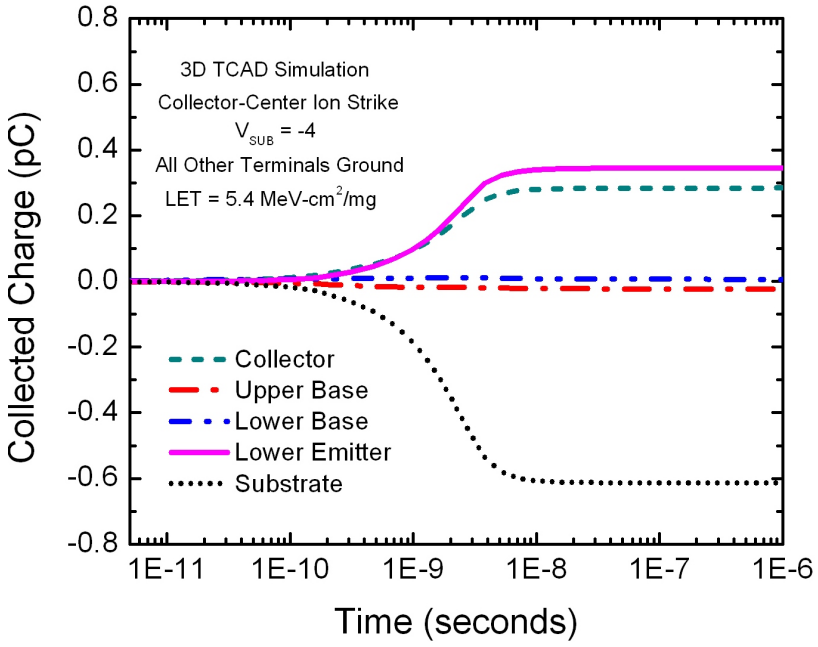

Figure 4.10: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 1.

observed (not for absolute charge collection values, but for the physical response of the device). In the current waveforms of Figure 4.9, several interesting points emerge. The first is that at very short times ($< 10^{-11}$ seconds) the emitter terminal shows very small perturbations in the current (voltage). Similarly, the collector terminal has a very large spike in transient current. These observations are resulting from the choice of strike ion strike location (center of the electrical collector). Since no charge is directly deposited in the emitter-lower base junction, there will not be a large perturbation as seen for the collector terminal. The second piece of information that can be extracted is that the original interpretation of the experimental charge collection data, namely reduction of charge collection on the collector terminal arising from charge sharing between the emitter and collector terminals, is supported. As illustrated in Figure 4.9, both the electrical collector and emitter have current plateau tails, of equivalent magnitude. When this current is integrated, it results in an equivalent amount of charge on both terminals, as illustrated in Figure 4.10.

Finally, the inverse-mode cascode SiGe HBT incorporating a biased C-Tap terminal was also simulated for an ion strike scenario. The location of the C-Tap terminal is depicted in Figure 4.6, and provides an electrical contact to the buried subcollector. The resulting current transient waveforms for all terminal and integrated charge profiles are shown in Figure 4.11 and Figure 4.12 respectively.

Once again the simulations are a reflection of the measurement results obtained. As can been seen in Figure 4.11, the presence of a C-Tap with applied bias results in nearly all electrons exiting through the C-Tap terminal. The only charge with is induced on the electrical collector terminal is due to the charge deposited directly within the depletion of the collector-upper base terminal. This is reflected in the collector current waveform of Figure 4.11, which shows only non-zero current directly following the ion strike event. Charges which are collected by the subcollector-substrate junction are able to be effectively removed by the C-Tap terminal. This result suggests that

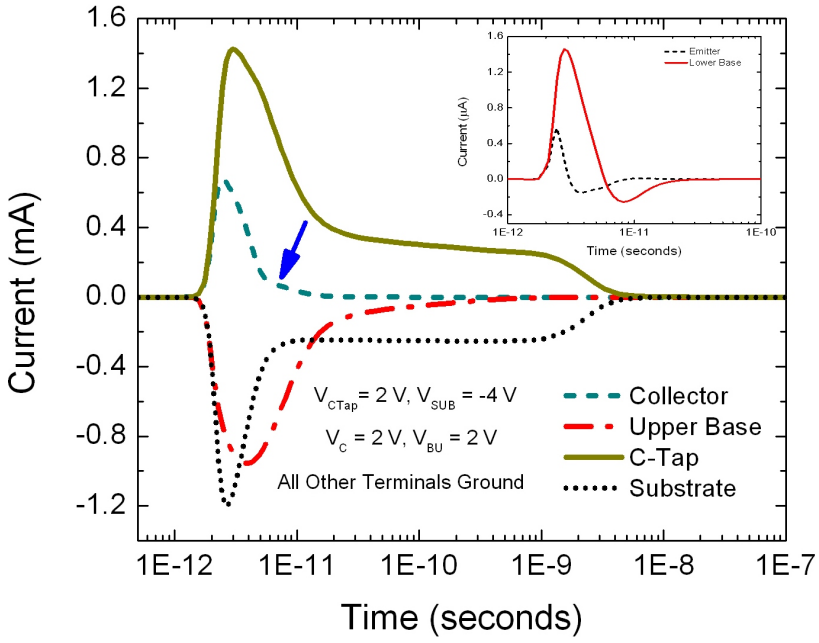

Figure 4.11: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT with C-Tap as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

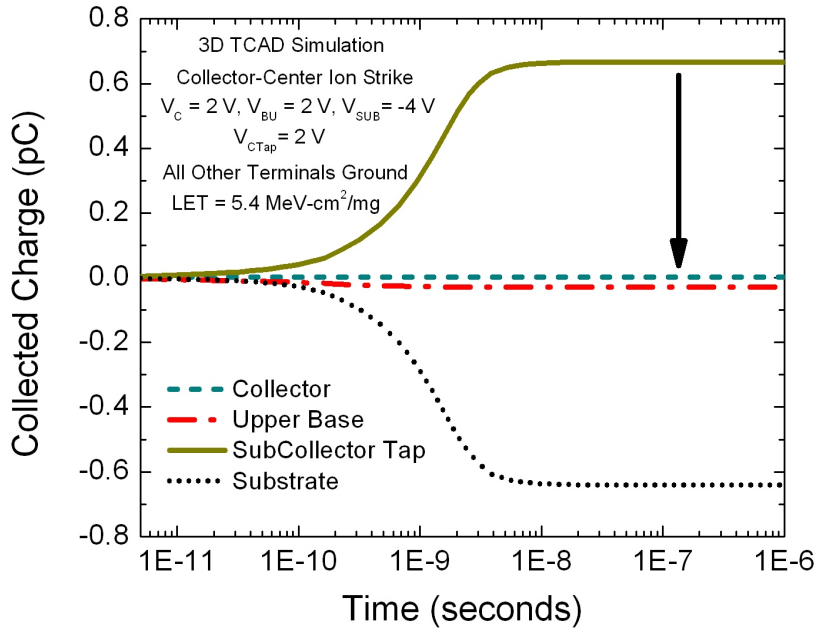

Figure 4.12: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT with C-Tap as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

by having a conductive electrical path out of the buried subcollector will provide significant SEU mitigation; however, complications arise when one considers how to effectively do this without comprising the operation of the inverse-mode cascode SiGe HBT.

4.7 Biasing the C-Tap Terminal

It has been shown that incorporating an electrical contact to the buried subcollector of the inverse-mode cascode SiGe HBT has the potential to offer incredible improvement in charge collection (SEU susceptibility) characteristics of the novel device. This conductive path from the buried subcollector to a rail is not a simple fix. The potential on the subcollector node changes dynamically, adjusting itself to correctly bias the upper transistor (Q2) of the cascode, based on the current state of the lower transistor (Q1). Recall that transistor Q2 essentially acts as a unity-current gain amplifier, where the input is the buried subcollector (the output of transistor Q1); therefore, the subcollector cannot be directly tied to a DC bias, as the bias point needs to dynamically change during device operation. Several concepts were developed to address this C-Tap bias concern, including a dynamically controlled FET conduction path to a rail and capacitive coupling to a rail. Given the simplicity of using a capacitor to tie the buried subcollector node to a rail voltage, this method has been investigated as a possible solution.

In order to theoretically verify the approach, Spectre simulations were employed. To represent the inverse-mode cascode structure with a subcollector node capacitively coupled to a rail, the schematic in Figure 4.13 was implemented.

The HBT devices used were two discrete standard structures, with transistor Q2 operated in inverse-mode and transistor Q1 operated in forward mode. This allowed the device models in the spectre environment to be utilized, given that the novel device has no operational models associated with it. To simulate the effects of

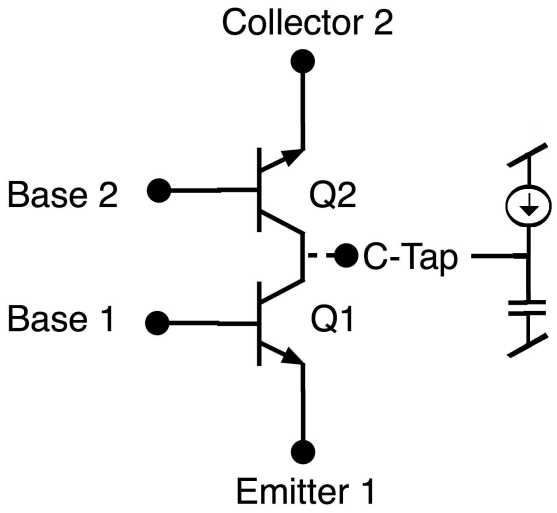

Figure 4.13: Schematic of the inverse-mode cascode SiGe HBT with capacitive coupling on the buried substrate. Transient current waveforms were injected on the subcollector terminal and measured at the output node.

capacitive coupling on the transient current waveform at the output node (Collector 2), a current source was tied to the subcollector node of the cascoded pair. This current source was programmed to inject the C-Tap transient current waveform that was generated using the ion strike simulation in NanoTCAD from Figure 4.11. A transient

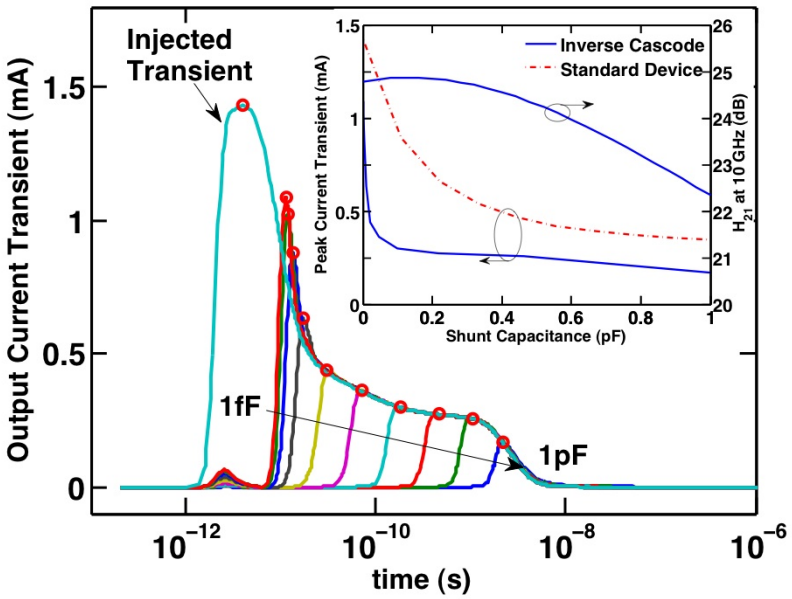

Figure 4.14: Simulated current transients on the output terminal for varying capacitor values on the buried subcollector node.

simulation was then executed in spectre, while the cascoded pair operated in the off state (the previously defined bias scheme 2). Multiple simulations were run with varying capacitor values, the results of these simulations are presented in Figure 4.14. As evidenced by the simulations, capacitive coupling serves as an effective means of eliminating the current transient from reaching the output terminal. The mitigation of output current transient increases with an increase in the capacitor value (understood as lower frequency components become filtered with larger capacitor values). The maximum speed of a CML digital cell is expected to drop as the capacitor increases in size, so a trade-off exists between system speed and amount of SEU mitigation acquired.

CHAPTER V

CONCLUSION

5.1 Topical Review

The purpose of this thesis was to investigate two radiation hardening by design techniques that are proposed for SiGe BiCMOS technologies. Both experimental data encompassing both total ionizing dose data and charge collection statistics from a heavy ion microbeam were utilized to explore the possible SEU mitigation offered by these techniques. The results and analysis that have been presented are a first look into the possibility of using these techniques for radiation hardening SiGe transistors for space applications. Although the preliminary investigations have uncovered promising potential for these techniques, a deeper analysis is required, as will be outlined in the future work section.

In Chapter 1, SiGe BiCMOS technology was introduced as a viable platform for incorporation in extreme environment application encompassing both low-temperature and large radiation fields. The fundamental differences between a pure silicon platform, and a silicon-germanium heterojunction bipolar transistor were discussed. A look into the benefits of bandgap engineering in a silicon system, through building and integrating SiGe alloys was also presented. The boosts in device operation from this bandgap engineering were also addressed. The inherent excellent low-temperature operation of SiGe HBTs was highlighted, and a preliminary look at the radiation tolerance of the technology was provided, focusing specifically on the SEE sensitivity of this technology.

Chapter 2 introduced the radiation environments which exist in space, by discussing the radioactive particle sources and elemental compositions of those fields. The effect

of these particles on semiconductor systems was then discussed in the context of total ionizing dose, displacement damage, and single event effects. The mechanisms behind each effect were addressed as well as the susceptibility of SiGe HBTs to each interaction. Given the susceptibility of SiGe HBTs to SEEs, a detailed overview of the origins of these effects were presented. Additionally, a look into previous work into radiation hardening this technology using both RHBD and RHBP techniques were discussed. This motivated the purpose of this thesis, to discover new RHBD techniques on the device-level to avoid the high area/power penalties paid for by current RHBD techniques.

The first device-level RHBD technique was introduced in Chapter 3, namely, the reduction or complete removal of the DTI in SiGe BiCMOS technologies. It is found that although the DTI does provide isolation from charge collection arising from ion strike events occurring outside the active area of the device, the DTI confines carriers inhibiting ambipolar diffusion for ion strikes within the active area. This confinement results in an increase of charge being collected by the sensitive junction. This study was performed using two of IBM's 3rd generation platforms which had different deep trench depths. Both TID and charge collection irradiations were performed and supported by full 3-D TCAD ion strike simulations. Reduced sensitivity is found for ion strikes to the center of the device, while increased charge collection events occur for strikes outside of the active area when compared to standard devices.

In Chapter 4, a novel device architecture was proposed for the purpose of mitigating SEEs. This topology encompasses two transistors connected in a cascode fashion using a shared subcollector. By operating the upper device in inverse-mode, this structure can be treated as a single device (although twice the voltage headroom is required). Both total dose testing as well as SEE testing (through charge collection measurements) was performed to characterize the radiation response of this new device topology. The total dose tolerance was found to be typical for the SiGe process the

device was fabricated with and no degradation was found at typical bias values for circuit operation. The charge collection statistics revealed intricacies in the device response. For a standard inverse-mode cascode no significant mitigation to charge collection is observed; however, when the buried subcollector is externally biased almost no collected charge is measured on the output terminal of the device. Given that the buried subcollector has to be dynamically biased, the possibility of using capacitive coupling to a rail voltage was investigated. Simulations show that given a sufficient value of capacitor, almost all the charge is extracted from the buried subcollector terminal without being directed to the collector terminal.

5.2 Future Work

Although some promising RHBD techniques have been presented and analyzed through both experimental and simulation data, there is still a significant amount of work left to be performed before these techniques can be declared effective SEE mitigation methodologies. To this point, studies have only been performed on the device-level (both experiments and simulations) for both RHBD techniques. The next step in qualifying these techniques as effective is building functional CML circuits incorporating these RHBD strategies. A broadbeam ion test environment can then be utilized to obtained a bit error rate (BER, a metric for quantizing the amount of digital errors for a given particle fluence). The ultimate test for qualifying an RHBD technique is to compare the BER for a standard, non-hardened topology to the BER generated by the same circuit. In addition, more extensive modeling can be performed to understand and predict the effects of these hardening techniques, especially if a mixed-mode environment is employed.

The next steps in the investigation of deep trench isolation for SEU mitigation, is to fabricated and simulate structures with no deep trench that also incorporate junction isolation. Additionally, these structures need to be integrated together to form a circuit

which will be compatible with BER testing. These structures have been designed and are currently in the process of being fabricated; additionally shift registers have been designed using junction isolated devices with the DTI removed. Once the hardware has been returned and proved to be functional, additional microbeam and broadbeam testing will be performed.

For the novel inverse-mode cascode SiGe HBT, a seemingly endless amount of research needs to be completed. Given that these are brand new structures, compact modeling should be performed, to allow circuit simulations to be run on designs incorporating these devices. To continue the work of qualifying these devices as a RHBD technique, structures must be fabricated incorporating the capacitive coupling of the buried subcollector to a rail voltage. These structures have been designed and will be measured and irradiated in a microbeam environment once fabricated. Also, a shift register circuit has been designed which incorporates these structures. This will be the first circuit implementation ever attempted using these novel devices. Provided correct functionality, these circuits will be tested in a broadbeam environment to generate a BER for this application.

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